1.0 Single Event Effects

1.1 SEE Scope

This report contains an assessment of the single event effects, total dose, and displacement damage performance for susceptible devices (LM124, LM139, LP2953, REF02A, 53124, and 53111) in the Monitor-OV Indicator board. The assessment was based on available test data from public domain and proprietary sources and used computed circuit bias conditions. Upset rates were estimated for Geostationary Orbit (GEO) environment in CREME96 (https://creme96.nrl.navy.mil/) using standard methods and procedures for rate estimation. It should be noted that this assessment is applicable to the specific vendor of the part. It is known that different vendors of the same part type give different radiation responses.

Analysis:		**Radiation Analysis**	
Performed by:		**MS/CH**	
Last Rev Date:		**6/22/2009**	
Assembly:			
Schematic:			
BOM File			
Comply: Anticipated		**Radiation Analysis Summary**	
Parameter	**Requirement**	**Requirement**	**Compliance**
TID	**200kRAD**	**All devices suffer degradation and/or functional issues**	**w/Shielding**
DD	**4E+11**	**Some devices suffer degradation**	**w/Shielding**
SET		**<1E-3 per year**	**Meets**
SEU		**Cell-Error Rate of <1E-10 errors/cell-day and a LET of >75 MeV-cm^2/mg**	**N/A**
SEL		**LET > 75 MeV-cm^2/mg**	**Meets**
SEB		**LET < 35 MeV-cm^2/mg**	**Meets**
SEGR		**LET < 35 MeV-cm^2/mg**	**Meets**

Note: TID and DD requirements are 2x those derived from Customer provided data and obtained from 100mil shielding data points.

1.2 SEE Performance

The components susceptible to SEE were evaluated for Single Event Transient (SET). A summary of the SEE results are shown in Table 1.

Table 1. Summary of Single Event Effects Assessment

Part Number	Description	Manufacturer	Max. SET Duration (usec)	Max. Amplitude (V)	Upset Rate (upset/device-day)	Comments
5962R9950402VZA	IC, Quad Op. Amp., LM124QML	National Semiconductor	23	Rail-Rail	3.00E-02	+0.5V (positive SETs)
5962R9673802VXA	IC, Comparator, Quad, LM139QML	National Semiconductor	4	Rail-Rail	2.00E-05	+2V (positive SETs)
5962R8551401VPA	IC, V Ref., 5V, REF02AZ/QMLR	Analog Devices	10	Rail-Rail	2.80E-04	+10V (positive SETs
"	"	"	10	Rail-Rail	2.80E-04	-1.6V (negative SETs)
"	"	"	10	Rail-Rail	1.10E-03	-3.8V (negative SETs)
5962-9233601QXA	IC, Regulator, Adjustable, LP2953AMWG-QMLV	National Semiconductor	20	Rail-Rail	4.00E-03	Assumed SET duration
53124-110	IC, Solid State Relay, 1.6A DC	Micropac	none		<1E-7	
53111-110	IC, Solid State Relay, 1.6A DC	Micropac	none		< 1E-7	

Other Effects:

1) The parts are not susceptible to single event latch-up (SEL) to a LET of 90 MeV-cm2/mg.

2) The MOSFETs in the 53124 & 53111 are not susceptible to SEB or SEGR at any LET level at the operating VD voltage of 4.3V. MOSFETs derated below 25% of their rated VDS voltage are known not to be susceptible to SEB or SEGR.

1.3 Functional Descriptions

The differential amplifier consists of resistors and an LM124 amplifier. This circuit has a gain of 0.301 and is replicated several times.

The output of each differential amplifier is filtered and then compared with a reference voltage, derived from a precision 5V reference and a resistor divider at each comparator. The comparison is made using an LM139 comparator for each cell and the outputs of all of the LM139's are connected together to provide a single overvoltage detection level. The LM139 circuits include hysteresis to prevent chattering or oscillations of the overvoltage signal.

The LM139 combined output is then used to provide an overvoltage signal to an optically coupled solid state relay. The solid state relay output is then an isolated Mosfet Drain Source signal.

1.4 SEE Analysis Results

Note: the references refer to the listing in section 3.1, SEE References

LM139 (5962R9673802VXA):

The LM139 is a quad comparator manufactured by National Semiconductor. The pin out diagram is shown in Figure 1. In the application, two comparators are used, U1C (pins 10/11) & U1D (pins (8/9). In the application, U1 & U2 are biased with a single source of 12 volts. The differential input voltage is 1.3V in non-inverting mode.

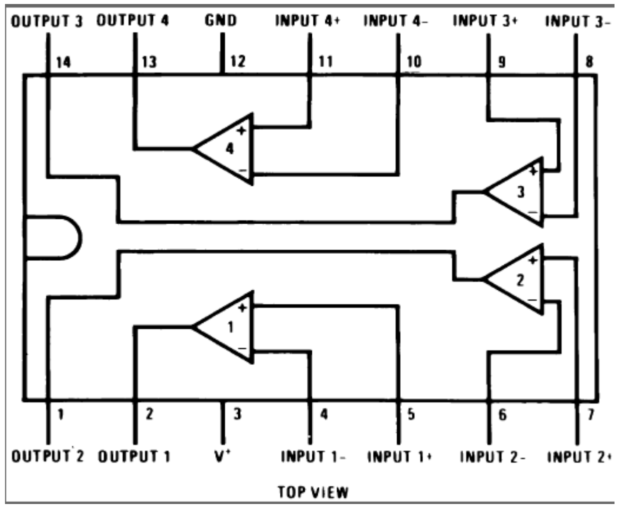

Figure 1. LM139 Connection Diagram

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Figure 2. LM139 Application Circuit

The LM139 is known to be susceptible to single event transient (SET) upsets. Positive SETs are expected for a positive supply voltage and positive and negative transients are expected from a dual source bias. SET amplitude and duration are dependent on the differential input and supply voltages. Figure 3 (Ref. 1) shows a sample of the distribution of pulse characteristics (amplitude & width). Note that the maximum SET duration here is 3 usec and the amplitude ranges from a few mV to rail to rail. In other tests, the maximum observed SET width of all the runs is ~ 4.0us (trigger voltage was set to 2V).

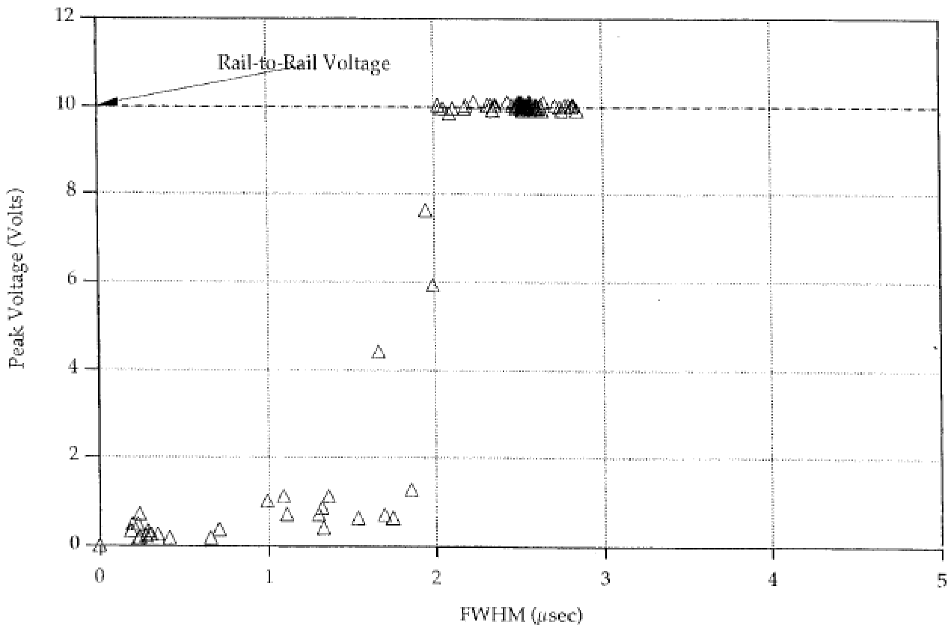

Figure 3. Sample of the pulse characteristics distribution for an irradiation run (Ref. 1)

Heavy ion test data was obtained from the literature (Ref 2). Figure 4 shows the SET characteristics for several differential voltages and for +13v supply voltage; the part sensitivity increases as the differential voltage decreases. In the application, the differential voltage is 1.3V. Since no data is available at 1.3V, and as a worst case, we used the data for 1.17V. The data represents all SETs with amplitude > 2V and all durations. This data was used to calculate the upset rate for the LM139.

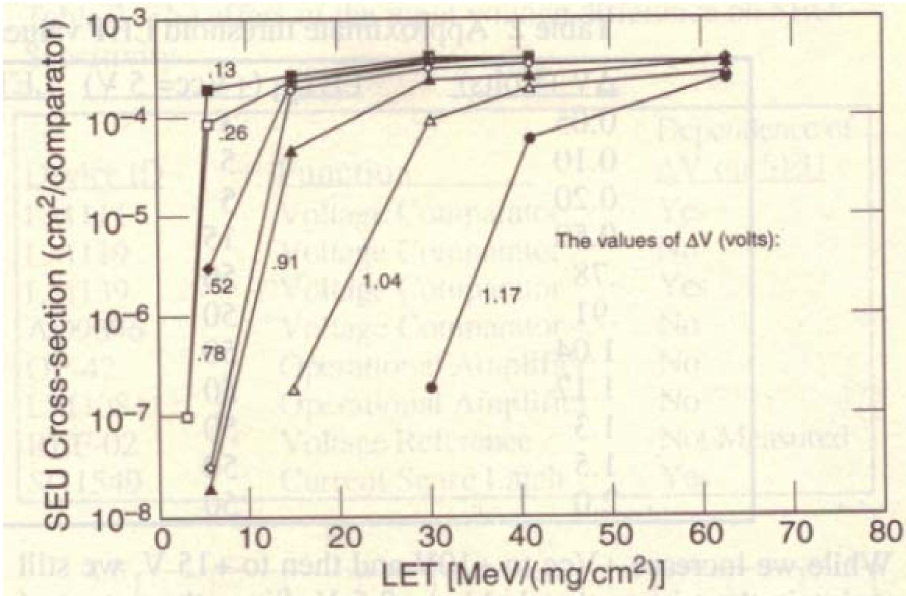

Figure 4. SET Characteristics at various differential voltages for +13V supply (Ref. 1)

Three standard methods are used in rate estimation; in the first method, the test data is fitted to a Weibull distribution function. Weibull parameters are calculated using Eq.1.

$$W(L) = 1 - \exp\left[- \left({(L - L_o)}/{w} \right)^p \right] \qquad (1)$$

Here, L_o, w, and p are the onset LET, width, and power of the Weibull distribution function.

These parameters are used as inputs to the rate estimation code in the CREME96 (https://creme96.nrl.navy.mil/) model. Upset rates are then calculated for solar minimum conditions (as a worst case in the solar cycle) and 200 mils shielding.

The 2nd method uses the HICUP (Ref 3) model, which also requires a good set of test data and was not used here. This method is recommended for critical upset rate estimation.

Since there are only 3 data points, and for worst case calculations, we used the 3rd method for rate estimation i.e. Peterson's Figure of Merit (PFM), as shown in Eq. 2. This model approximates the SET characteristics to a step function, which is a worst case condition. A

Modified PFM model assumes a K factor of a 100 was used; this value of the 'K' factor was derived with flight data.

From Figure 2, the saturated cross section for the LM139 is 2.0E-4 cm^2 and the Linear Energy Transfer (LET) threshold is 30 MeV-cm^2/mg.

$$R \approx K * \frac{\sigma_{sat}}{Lc^2} \quad (2)$$

Where R is the upset rate in events/comparator-day, K is a constant, σ_{sat} is the saturated cross section in cm^2 and Lc is the LET threshold (the lowest LET at which upset is first observed).

$$\sigma_{sat} = 2.0\text{E-4 cm}^2$$

$$Lc = 30 \text{ MeV-cm}^2/\text{mg}$$

Hence the worst case upset rate is 2.0E-5 upsets/comparator-day OR 2083 years/upset per comparator. This is consistent with available but unpublished flight data off several satellites. Flight data shows an upset rate of ~ 8.0E-5 upset/comparator-day for devices with 1.0 volt differential voltage. Hence, for differential voltage of 1.3v, the SET rate is expected to be lower ~ 2.0E-5 upsets/comparator-day. SET duration ranges from a few nanoseconds to a maximum of 4 microseconds. The part is not susceptible to single event latch-up (SEL).

LM124QML (5962R9950402VZA):

The LM124 is a quad operational amplifier (Op Amp) manufactured by National Semiconductor. The device pin out is shown in Figure 5. In the application, eight Op Amps are used with supply voltage of 12 volts. The input voltage of the 1st Op Amp is 1, and the next one is 2V, etc; the last one has approximately 8 volts input.

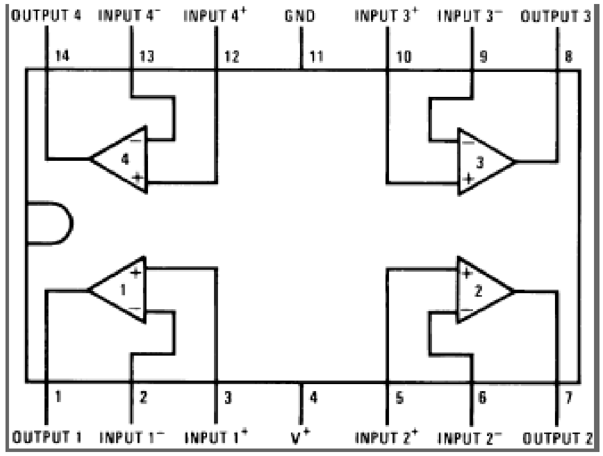

Figure 5. LM124 Connection Diagram

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Figure 6. LM124 Circuit Application Diagram

The LM124 is known to be susceptible to single event transient (SET) upsets (Ref 1 & 4-8). Positive SETs are expected for positive supply voltage. SET transient amplitude and duration are dependent on both input and supply voltages. Figure 7 (Ref. 4) shows a sample distribution of pulse characteristics (amplitude & duration). The maximum observed SET width of all the runs is ~ 23.0 usec and amplitude ranges from a few mV to rail to rail.

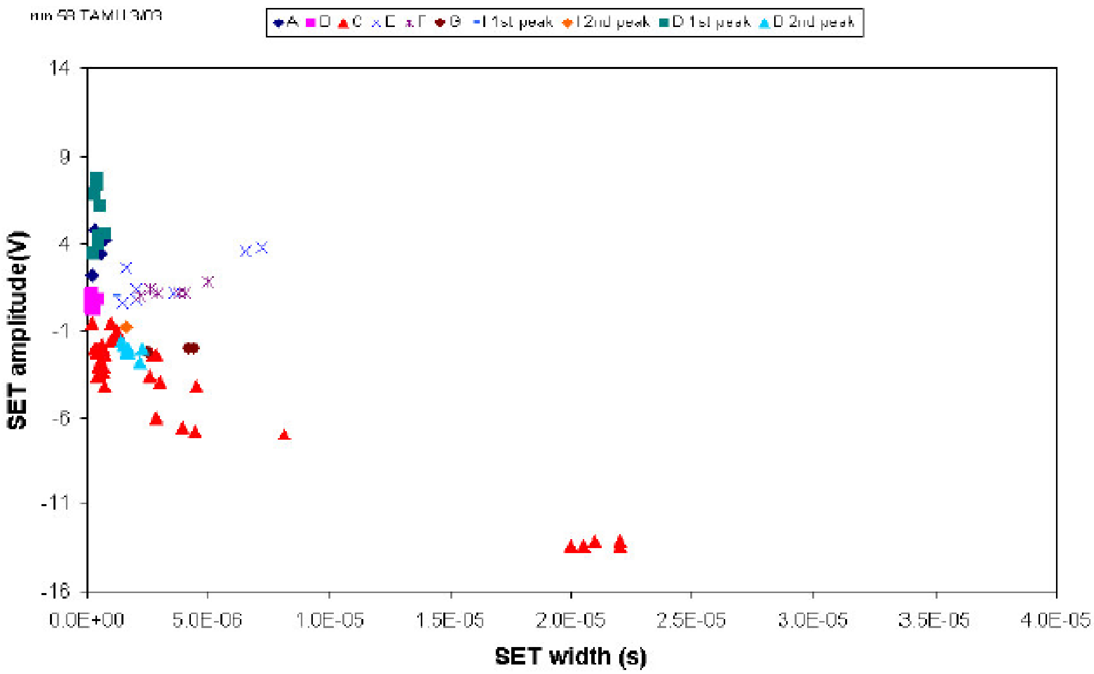

Figure 7. SET amplitude vs. duration (Ref 4)

Heavy ion test data was obtained from the literature (Ref 4). Figure 8 shows the SET characteristics for several input voltages for +12V supply voltage and for various input voltages. It is clear that the input voltage is not a strong function of the SET cross section; however, it impacts the SET characteristics (amplitude and duration). In our application (Figure 6), the input voltage for the first stage is 1.0V and output voltage is 1.2 volts. So this data can be used to estimate the upset rate for our application.

As a worst case, we will assume the maximum SET amplitude is rail to rail and the maximum duration is 23 usec.

From Figure 8, the upset LET threshold is ~ 3 MeV-cm^2/mg and the saturated cross section is 3.0E-3 cm^2 (for SETs >500 mV).

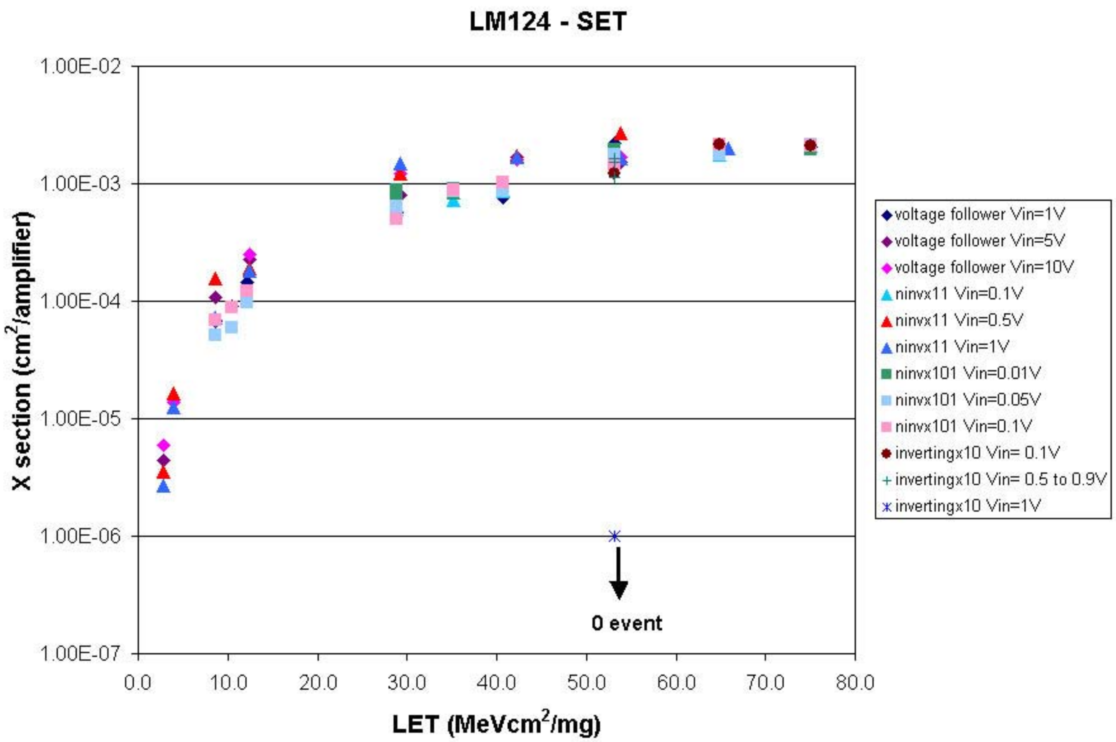

Figure 8. LM124 SET cross-section curves for different bias conditions (Ref. 4).

The Peterson's Figure of Merit (FOM) in Eq. 2 was used to estimate the worst case upset rate. The saturated cross section was taken to be 3.0E-3 cm^2 and the Linear Energy Transfer (LET) threshold is 3.0 MeV-cm^2/mg.

$$R \approx K * \frac{\sigma_{sat}}{Lc^2}$$

$$\sigma_{sat} = 3.0\text{E-}3 \text{ cm}^2$$

$$Lc = 3.0 \text{ MeV-cm}^2/\text{mg}$$

Hence the <u>worst case upset rate is 3.0E-2 upset/Op Amp-day</u>. For eight Op Amps, the upset rate is 2.4E-1 upset/day or ~ 88 upsets/year. The part is not susceptible to single event latch-up (SEL).

REF02AZ/QMLR (5962R8551401VPA):

The REF02 is a 5V reference voltage manufactured by Linear Technology. The application circuit is shown in Figure 9. The input voltage is 12V and the output is 5V.

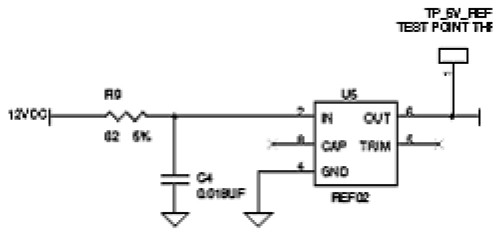

Figure 9. REF02 Circuit application diagram.

The SET upset cross section vs. LET (Ref 2) for different trigger threshold values (1.6, 3.8, and 10 volts) are shown in Figure 10. The SET characteristics are dependent on the trigger voltage; hence, its effect on the upset rate. There is no data on the duration of SET transients; however, a similar part, REF43's maximum recovery time is 10 usec (Ref. 4).

A wide range of pulse heights was observed, both positive and negative, from the nominal quiescent 5V output. However, there were substantially more transients with a smaller amplitude than those with a larger amplitude (Ref 2).

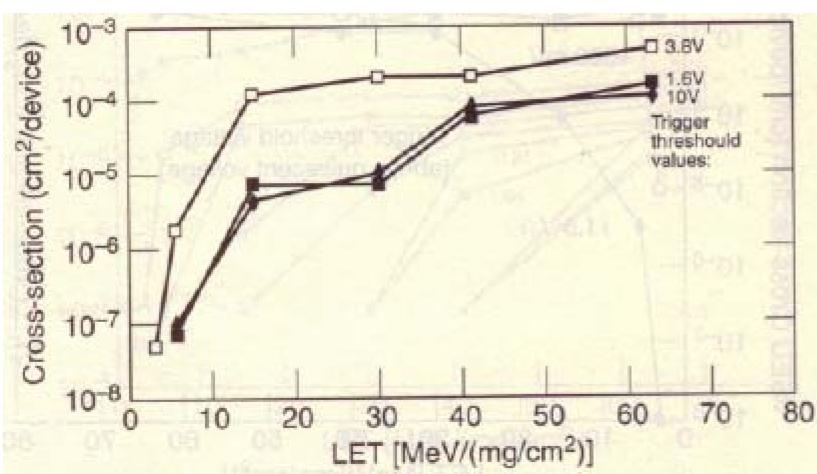

Figure 10. SEU test results for REF-02 for varying threshold voltage (Ref 2).

The LET threshold is ~ 3 MeV-cm^2/mg and the saturated cross section is 1.0E-4 (for positive SETs with a trigger voltage of 10V and negative SETs with trigger voltage of 1.8V) and ~ 8.0E-4 cm^2 for negative transients and a trigger voltage of 3.8V.

The Peterson's Figure of Merit (FOM) is used to estimate the worst case upset rates.

a- SET Rate for Positive SETs with Threshold Set at 10V:

The saturated cross section is 1.0E-4 cm^2 and the Linear Energy Transfer (LET) threshold is 6.0 MeV-cm^2/mg. Using Eq.1:

$$R \approx k * \frac{\sigma_{sat}}{Lc^2}$$

$$\sigma_{sat} = 1.0\text{E-}4 \text{ cm}^2$$

$$\text{Lc} = 6.0 \text{ MeV-cm}^2\text{/mg}$$

Therefore, the <u>worst case upset rate is 2.8E-4 upset/device-day</u> or ~ 10 years/upset in per device.

b- SET Rate for Negative SETs with Threshold Set at 1.6V:

The saturated cross section is 1.0E-4 cm^2 and the Linear Energy Transfer (LET) threshold is 6.0 MeV-cm^2/mg. Using Eq.1:

$$R \approx k * \frac{\sigma_{sat}}{Lc^2}$$

$$\sigma_{sat} = 1.0\text{E-}4 \text{ cm}^2$$

$$\text{Lc} = 6.0 \text{ MeV-cm}^2\text{/mg}$$

Therefore, the <u>worst case upset rate is 2.8E-4 upset/device-day</u> or ~ 10 years/upset in per device.

c- SET Rate for Negative SETs with Threshold Set at 3.8V:

The saturated cross section is 8.0E-4 cm^2 and the Linear Energy Transfer (LET) threshold is 3.0 MeV-cm^2/mg. Using Eq. 1:

$$R \approx k * \frac{\sigma_{sat}}{Lc^2}$$

$$\sigma_{sat} = 8.0\text{E-4 cm}^2$$

$$Lc = 3.0\ \text{MeV-cm}^2/\text{mg}$$

Therefore, the <u>worst case upset rate is 1.1E-3 upset/device-day</u> or ~ 2.5 years/upset per device. The part is not susceptible to single event latch-up (SEL).

LP2953AMWG-QMLV (5962-9233601QXA):

The LP2953 is an adjustable voltage regulator manufactured by National Semiconductor. The device pin out is shown in Figure 11. In the application, the opamp is biased with a single source of 12 volts. The input voltage of the 1^{st} opamp is 1, and the next one is 2V, etc; the last one has 8 volts input.

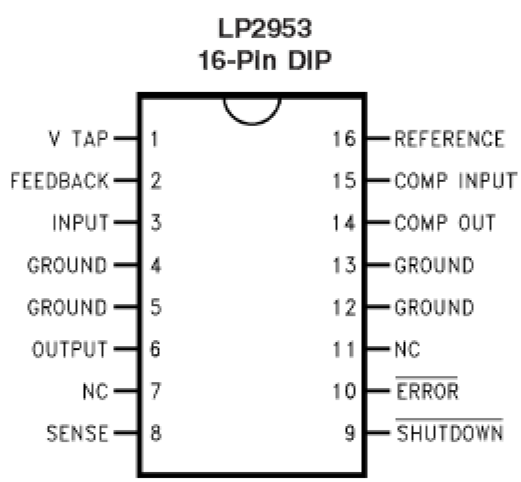

Figure 11. LP2953 connection diagram

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Figure 12. LP2953 circuit application diagram.

The **LP2953** is susceptible to single event transients (SET). Both positive and negative transients are expected.

Heavy ion upset test data (Ref 9) show a saturated upset cross section of 1.0E-3 and a LET threshold of 5 MeV-cm^2/mg.

The modified Peterson's Figure of Merit (FOM) was used to estimate the worst case upset rate.

$$R \approx K * \frac{\sigma_{sat}}{Lc^2}$$

$$\sigma_{sat} = 1.0\text{E-3 cm}^2$$

$$\text{Lc} = 5.0 \text{ MeV-cm}^2\text{/mg}$$

Therefore, the <u>worst case upset rate is 4.0E-3 upset/device-day</u>.

If better SET rate is required, testing will be required using application bias conditions.

SEL latch-up occurs in CMOS and ECL bipolar devices. SEL requires a 4-layer NPNP or PNPN structure; this structure forms two PNP & NPN transistor (usually parasitic but not always); the latchability of this structure depends on the current gain product of these two transistors (B1*B2=1 or higher). Of course temperature can increase the gain of the transistor making them more susceptible to latch-up. The LP2953 is a bipolar device and hence is not susceptible to SEL (generally agreed rule of thumb). In addition, there is proprietary data showing no latch-up to a LET of 90 MeV-cm^2/mg.

53124-110 (5962R9950402VZA):

The 53124 is a single channel power MOSFET opto-coupler manufactured by Micropac. The device pin out is shown in Figure 13 for DC connection. The application circuit is shown in Figure 14.

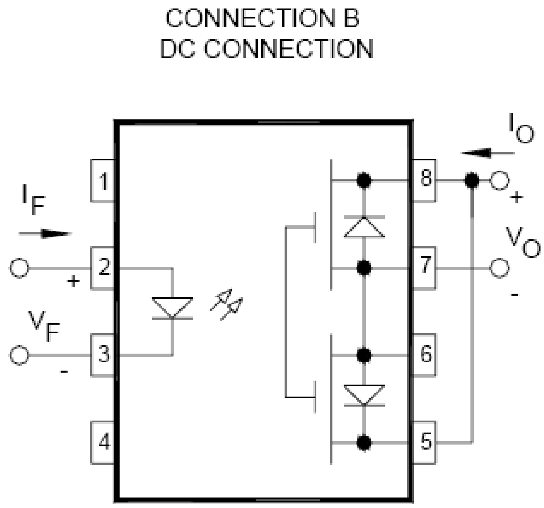

Figure 13. 53124 connection diagram

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Figure 14. 53124 circuit application diagram

Heavy ion test data, as shown in Table 2, was obtained from Ref 10. The 53124 is not susceptible to SETs but is susceptible to single event gate rupture (SEGR) as shown in Ref 11. Test data show SEGR threshold at LET of 37 at voltages of 70 volts.

Table 2. Heavy Ion Test Results*

Device	V_0 (V)	V_{LOAD} (Ω)	I_{EFF} (current if LED on)	SEGR	Max LET at this bias
53124	1.2	0.6	2A	No	59.9
53124	10	200	50mA	No	59.9
53124	10	1.25k	8mA	No	59.9
53124	30	1.8k	17mA	No	59.9
53124	30	11.25k	3mA	No	59.9
53124	50	5k	10mA	No	59.9
53124	50	31.25k	2mA	No	59.9
53124	70	9.8k	7mA	Yes	59.9
53124	70	61.25k	1mA	No	59.9
53124	90	17k	5mA	No	59.9
53124	90	101k	0.9mA	Yes	59.9

*All exposures greater than 1E7 particles/cm^2

SEGR failure is dependent on a MOSFET's drain-to-source (VDS) voltage. The higher the voltage, the more susceptible a FET is to SEGR. The maximum application VDS voltage is 4.3 volts (Ref 12) and is < 5% of the part's rated voltage of 90V. Since there is a large margin from where the device failed (VDS=70V) and the application voltage (VDS=4.3V), this device is not susceptible to SEGR at the present application voltage. MOSFETs that are derated to 25% or lower of their rated VDS are not susceptible to SEB or SEGR.

The 53124 is not susceptible to SETs. The part is not susceptible to single event latch-up (SEL).

53111-110

Micropac 53111 is a one-channel power MOSFET opto-coupler hermetically sealed with an 8-pin ceramic DIP package.

There is no heavy ion SET data, however, test data (Ref 13) shows SEL and SEGR < LET of 83.4. There is proton test data at 63 MeV which shows no upset to a maximum fluence of 1E12. This is equivalent of saying no SETs to LET of 15 MeV-cm^2/mg.

The maximum application VDS voltage is 4.3 volts (Ref 12). Since there is a large margin from where the device failed (VDS=28 & 34V) and the application voltage (VDS=4.3V), this device is not susceptible to SEGR at the present application voltage. MOSFETs derated to 25% or lower of their rated VDS are not susceptible to SEB or SEGR. The part is not susceptible to single event latch-up (SEL).

1.5 Single Event Upset

SEU are upsets in mainly related to memory elements. There are no parts in the design that have memory elements. Therefore the design meets the requirement of a cell-error rate of < 1E-10 errors / cell-day and a LET of > 75MeV-cm^2/mg.

1.6 Summary of SET Impact

With respect to meeting the SET requirement of <1E-3 per year (assumes 100 mil nominal aluminum shielding) only single event upsets that impact performance of the unit are evaluated. Filtered upsets, upsets that have no impacts on the performance of the unit re not counted in the total upset rate of the unit.

Each of the SET conditions has been tested with the simulation results shown below. In each case, the upset time was applied. In some case the output was shorted to the input, in others the output was shorted to VCC or ground. The upset times are listed in Table 1 for each component. None of the SETs generate a change in the output state of the OV signal.

Figure Removed Due to Proprietary Information

Figure 15. SPICE implementation of the OV telemetry circuit including 12V regulator and 5V reference is used for SET simulations. Each model was independently tested and its simulation performance, relative to the requirements of this simulation, verified.

LM139

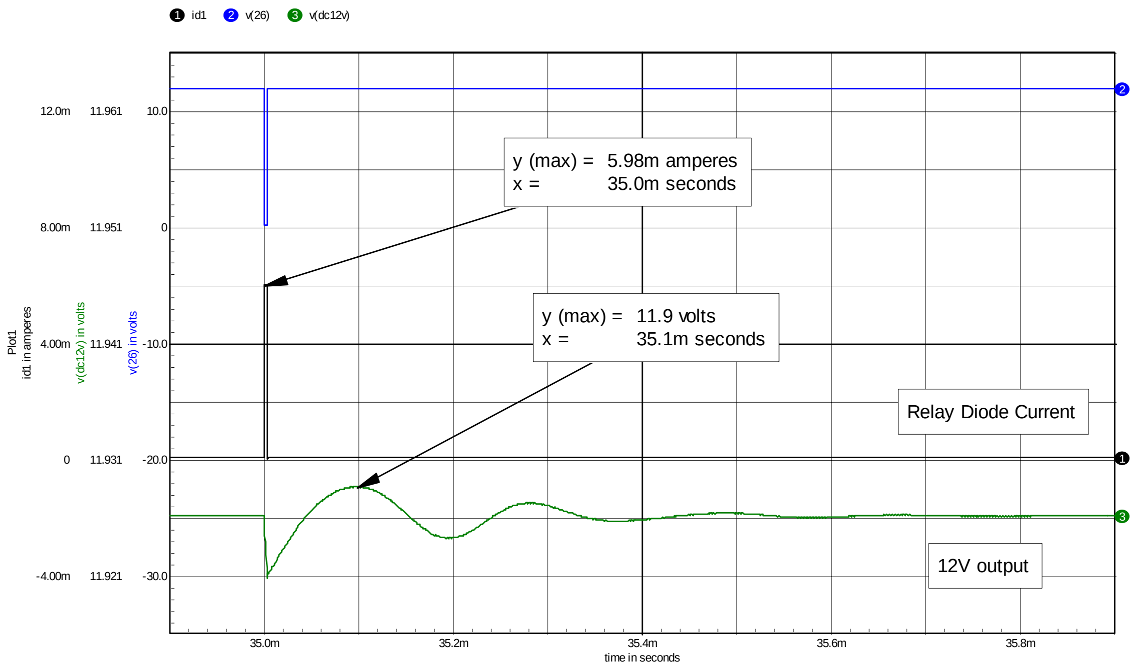

Figure 16. During the SET, the output of LM139 is shorted to the Vcc @35ms for 4us. The maximum relay input diode current is 5.98mA. The duration of the current pulse is extremely short and would not cause the relay to change state. The relay turn on time is on the order of 1ms.

LM124

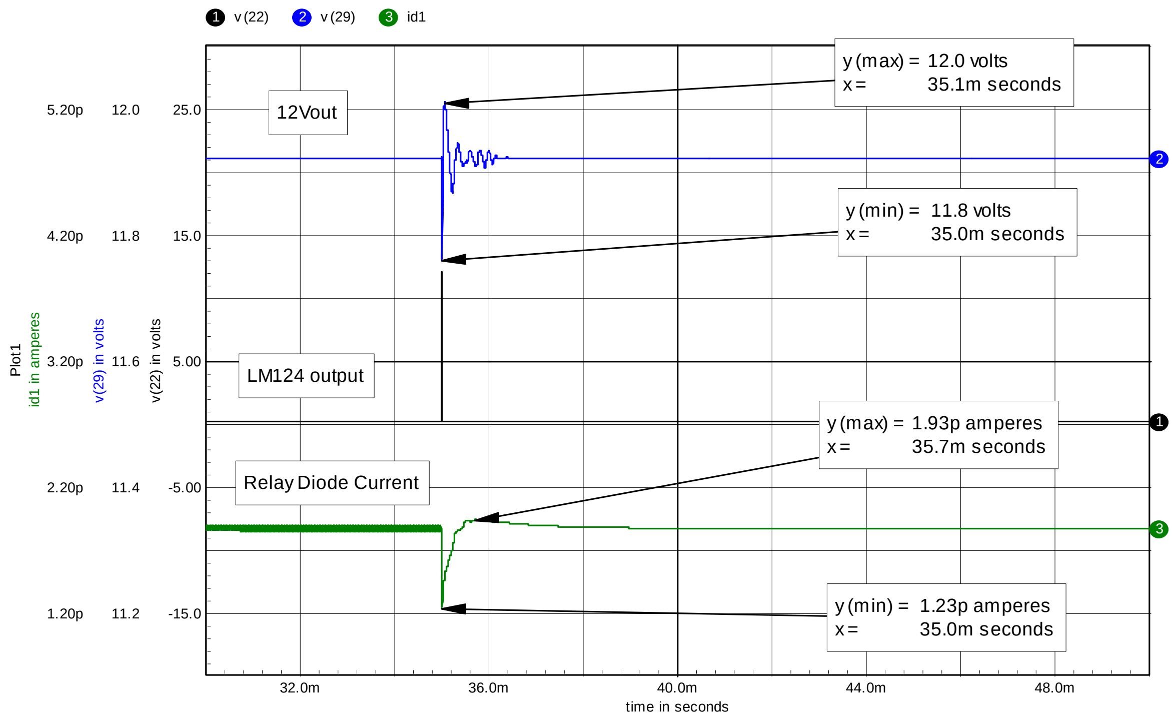

Figure 17. During the SET, the output of the LM124 is shorted to the Vcc @35ms for 23us. There is no significant impact on the relay diode input current.

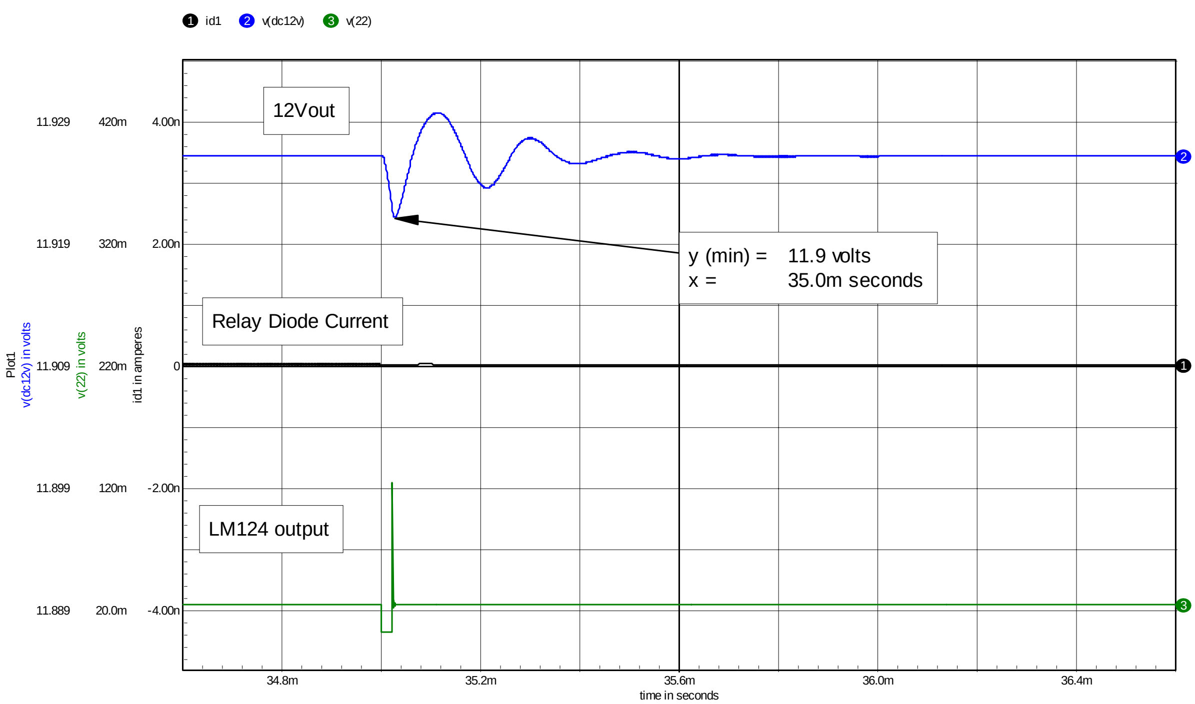

Figure 18. During the SET, the output of the LM124 is shorted to the ground @35ms for 23us. It does not have significant impact on the 12V reference or the relay current.

LP2953

The input and output can short during a SET. The INPUT pin is at VCC (24-34V minus the 10V zener voltage) and OUTPUT pin at 12V. During a SET, the 3.3uF input cap will discharge into the 4.7uF output cap as shown in Figure 19. During the event, the capacitors will continue to charge through the 10 ohm input resistor, and finally reaching a voltage of near 20V. No test data is available on the recovery time but the model was independently developed by AEi System and tested thoroughly against the data sheet for a wide variety of characteristics.

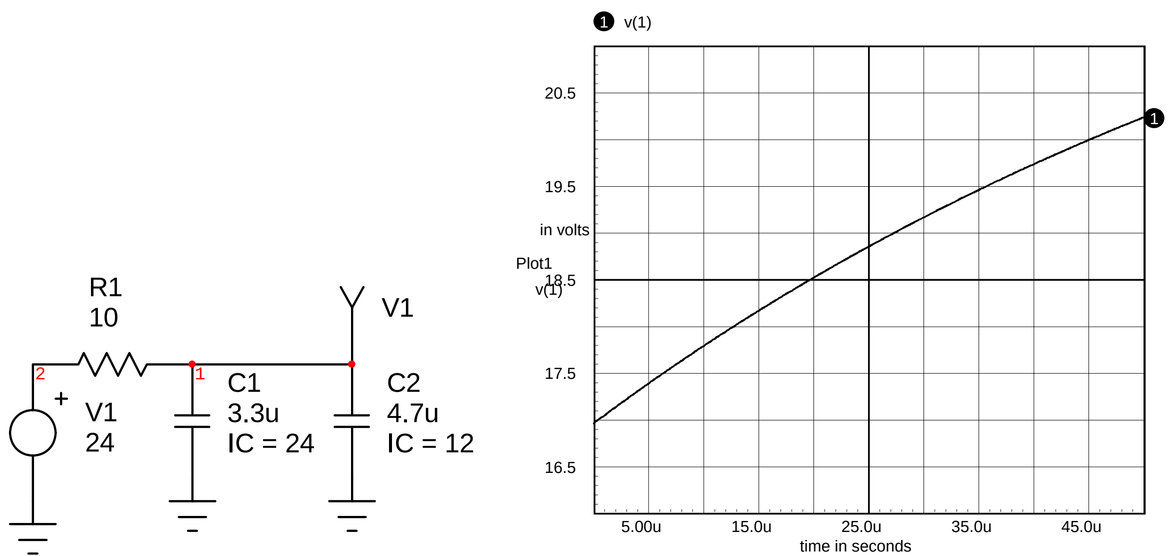

Figure 19. Assuming the input cap starts at 34V-10V=24V. The sum of the CV products has to be conserved. Therefore, 24V*3.3uF+12V*4.7uF=8uF*V. This would move the voltage at each cap to 17V (they have the same voltage, since they are shorted together). Now the caps continue to charge through the 10 Ohms.

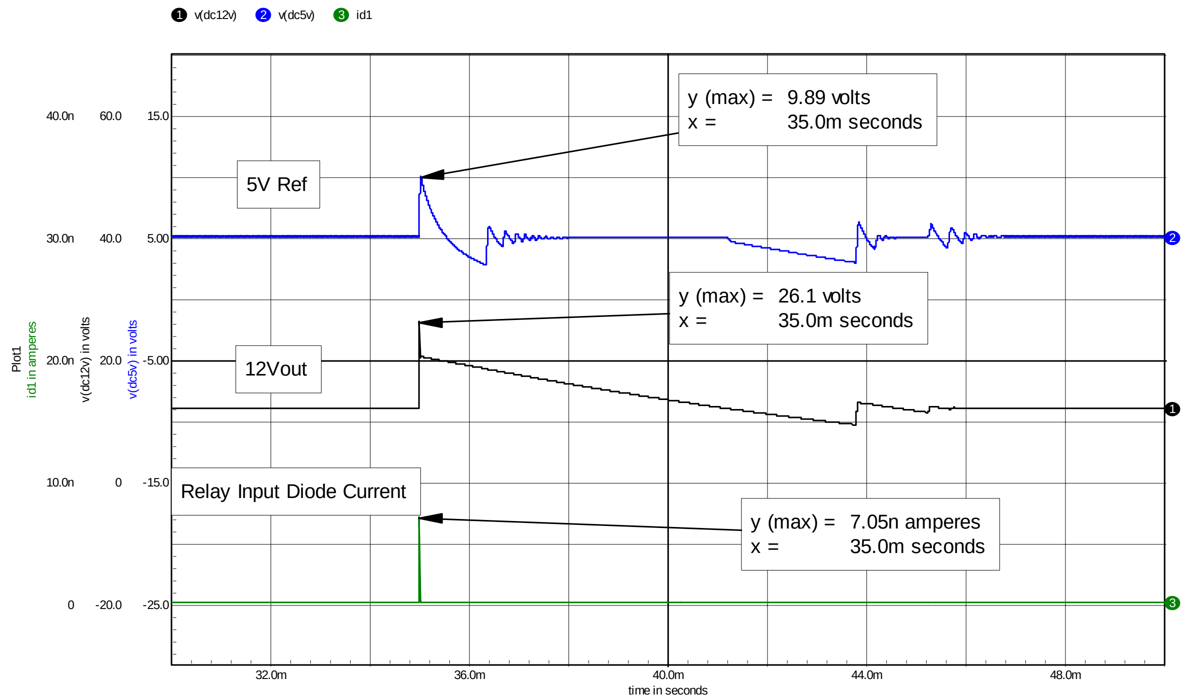

Figure 20. During the SET, the input and output of the LP2953A are shorted @35ms for 20us. The 12V output overshoots to 26.1V and 5V reference maximum is 9.89V. There are possible stress issues at the 5V reference and 12V output. The relay does not switch on due to this SET event.

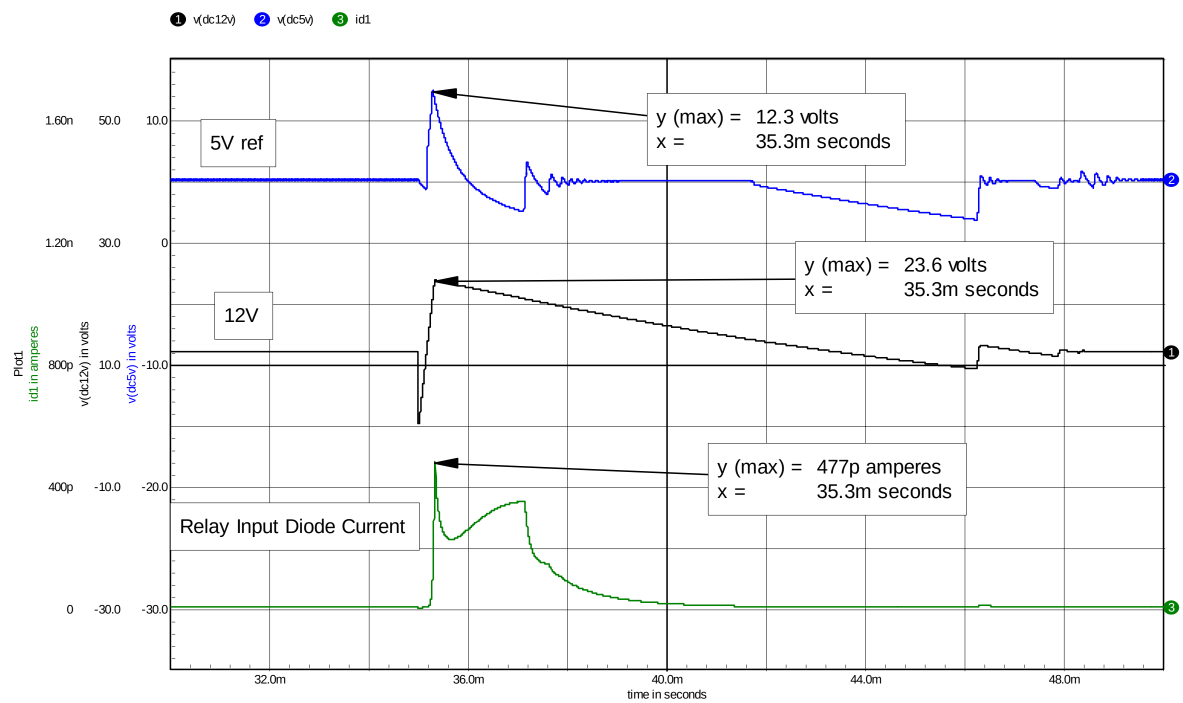

Figure 21. During the SET, the output of LP2953A is shorted to ground @35ms for 20us. The 12V output overshoots to 23.6V and 5V reference maximum is 12.3V. There are possible stress issues at the 5V reference and 12V output.

REF02

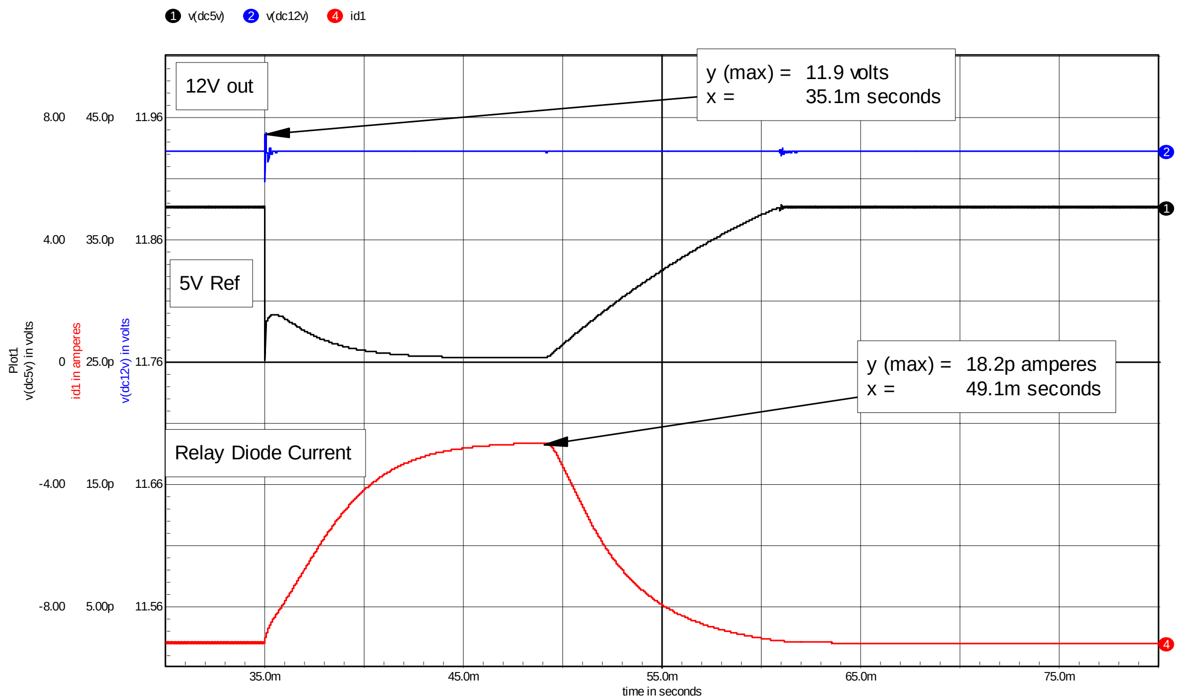

Figure 22. During the SET, the output of REF02 is shorted to ground @35ms for 10us. The 5V reference takes approximately 26ms to recover. The maximum relay diode current is 18.2pA which is insignificant.

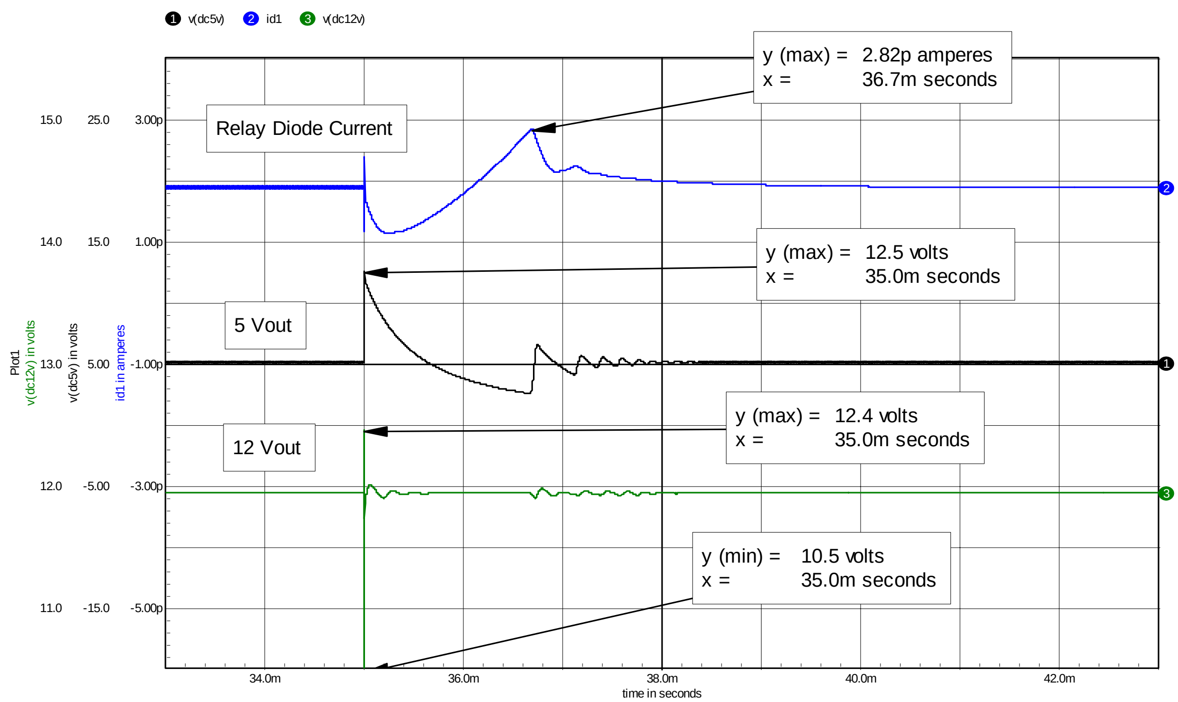

Figure 23. During the SET, the input and output of REF02 are shorted together @35ms for 10us. The 5V reference overshoots to 12.5V. The relay diode current does not have significant change.

2.0 TID AND NEUTRON FLUENCE EFFECTS

2.1 TID/DD Scope

This report contains total ionizing dose and displacement damage data for several devices (LM139, LM124, REF02, LP2953, 53124, and 53111). The assessment was based on available test data from public domain sources. Notably, this assessment is applicable only to the specific vendor of the part and for this application only. It is known that different vendors, lot-to-lot variations of the same part type to give different radiation responses. Table 3 contains a summary of the results.

Table 3. Summary of TID and DD Assessment.

Part Number	Description	Manufacturer	TID Functional failure (krad)	TID Parametric Degradation (krad)	Comments
5962R9950402VZA	IC, Quad Op. Amp., LM124QML	National Semiconductor	>125	See the SMD for post rad allowable shifts.	Displacement damage is insignificant. It is ELDRS free.
5962R9673802VXA	IC, Comparator, Quad, LM139QML	National Semiconductor	>100	See the SMD for post rad allowable shifts.	This device is sensitive to displacement damage. It is ELDRS free.
5962R8551401VPA	IC, V Ref., 5V, REF02AZ/QMLR	Analog Devices	>100	See the SMD for post rad allowable shifts.	Displacement damage is insignificant up to 2E12 neutrons/cm^2.
5962-9233601QXA	IC, Regulator, Adjustable, LP2953AMWG-QMLV	National Semiconductor	>30	Short circuit current degraded significantly	Part exhibits ELDRS. Displacement damage degraded short circuit current significantly
53124-110	IC, Solid State Relay, 1.6A DC	Micropac	> 300	Output leakage increased but remained within specs limits.	Displacement damage is insignificant for 63 MeV protons to an equivalent fluence of 2.5E12 neutrons/cm^2
53111-110	IC, Solid State Relay, 1.6A DC	Micropac	60	Remained within specs	Significant parametric degradation with 14 MeV neutrons

2.2 TID/DD Analysis Results

Note: the references refer to the listing in section 3.1, SEE References

LM139QML (5962R9673802VXA):

The LM139QML quad comparator is a 14 pin in CERPACK package manufactured by National Semiconductor. This new SMD version is guaranteed to 100 kRad and it is low dose rate (ELDRS) free.

Pre and post 100 kRad irradiation limits are identical to those listed in the part's specifications under AC and DC electrical characteristics except as listed Table 4 for 100 kRad.

Table 4. AC and DC electrical characteristics

DC/AC Parameters 100K Post Rad Limits +25°C (Notes 10, 14)

The following conditions apply, unless otherwise specified.

DC: +V = 5V, V_{CM} = 0V

AC: +V = 5V

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 5V, V_{CM} = 0		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 0		-4.0	4.0	mV	1
		+V = 30V, V_{CM} = 28.5V, V_O = 1.5V		-4.0	4.0	mV	1
± I_{Bias}	Input Bias Current	V_O = 1.5V	(Note 5)	-110	-1.0	nA	1
t_{RLH}	Response Time	V_{OD} (Overdrive) = 50mV			1.0	µS	4

Input bias current IB showed degradation due neutron irradiation of 20 nA at a fluence of 6.0E11 n/cm^2 which is much less than the total dose degradations of 110 nA. See tables 4 & 5. Therefore, the neutron effect here is insignificant.

In order to meet the 2x margin the part must be shielded with 120 mils Al or ~ 20mils of Tantalum. This will bring the total dose down to 53.8 kRad per mission.

For reference, older versions of the LM139 show significant parametric degradation at low total dose levels of 30kRad, as well as, Enhanced Low Dose Rate Sensitivity while SMD versions have insignificant degradation to 100 kRad, as shown in Figure 24 & 25. (ref. 2) and No ELDRS. Therefore, only this version 5962R9673802VXA is recommended with additional shielding, as noted above.

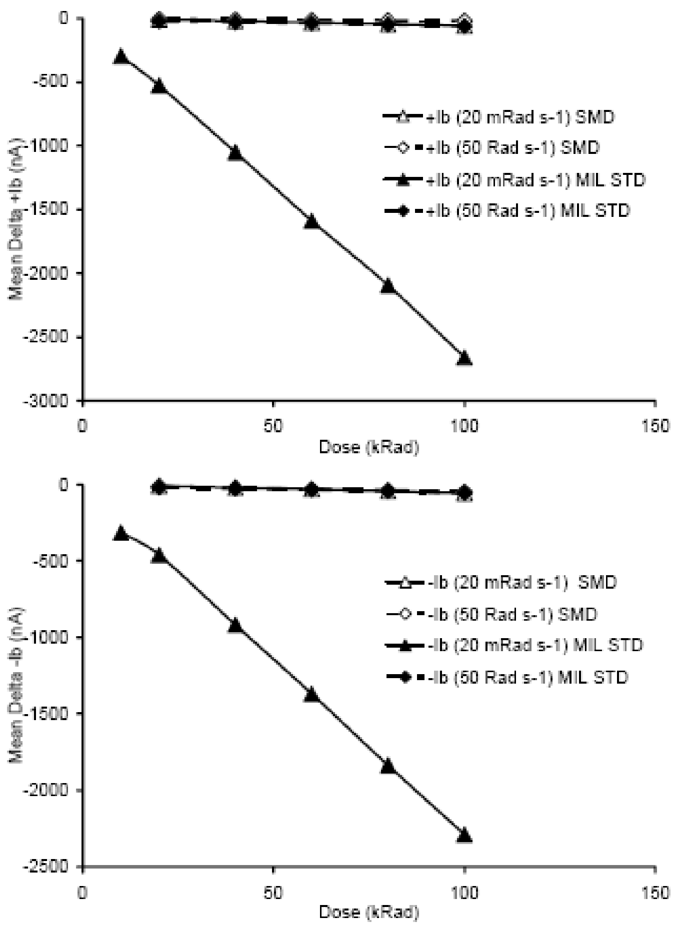

Figure 24. SMD and MIL-STD parts behavior with total dose

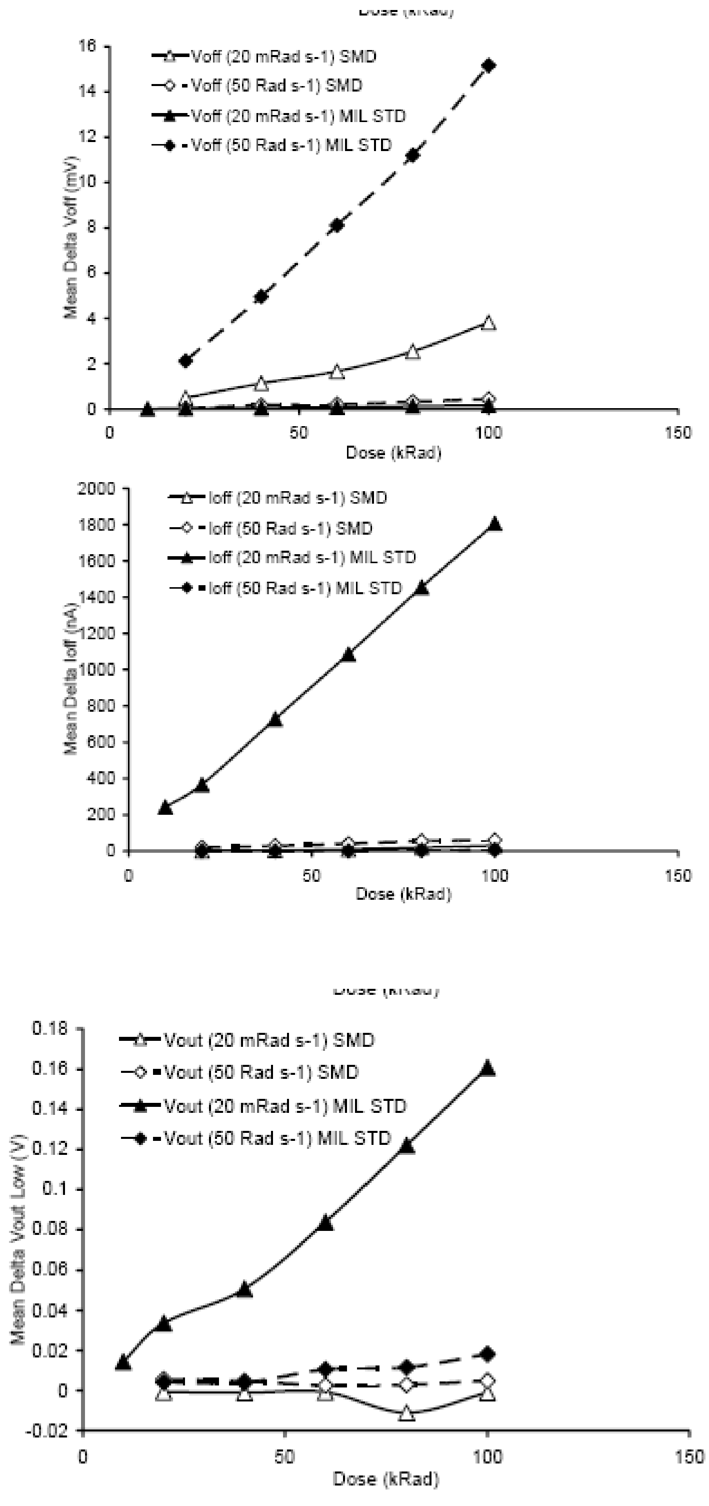

Figure 25. SMD and MIL-STD parts behavior with total dose

LM124QML (5962R9950402VZA):

The LM124QML quad operational amplifier (Op Amp) is a 14 pin in CERPACK package, with SMD specification #5962R9950402VZA, manufactured by National Semiconductor. This new SMD version is guaranteed to 100 kRad (pre rad limits) and > 125krad functional level (Ref 3) and it is low dose rate (ELDRS) free.

Pre and post 100 kRad irradiation limits are identical to those listed in the part's specifications under AC and DC electrical characteristics. (Ref 4). Input offset voltage versus total dose is shown in Figure 26.

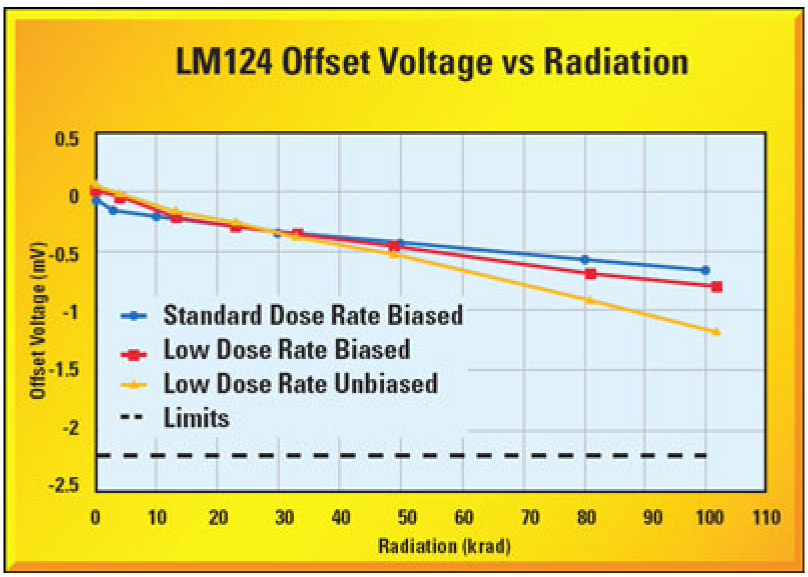

Figure 26. Offset voltage with total dose

Figures 27 shows mean delta IOS, delta +IB, and –IB for the SMD version and others. It is shown that these parameters have insignificant degradation below 100krad.

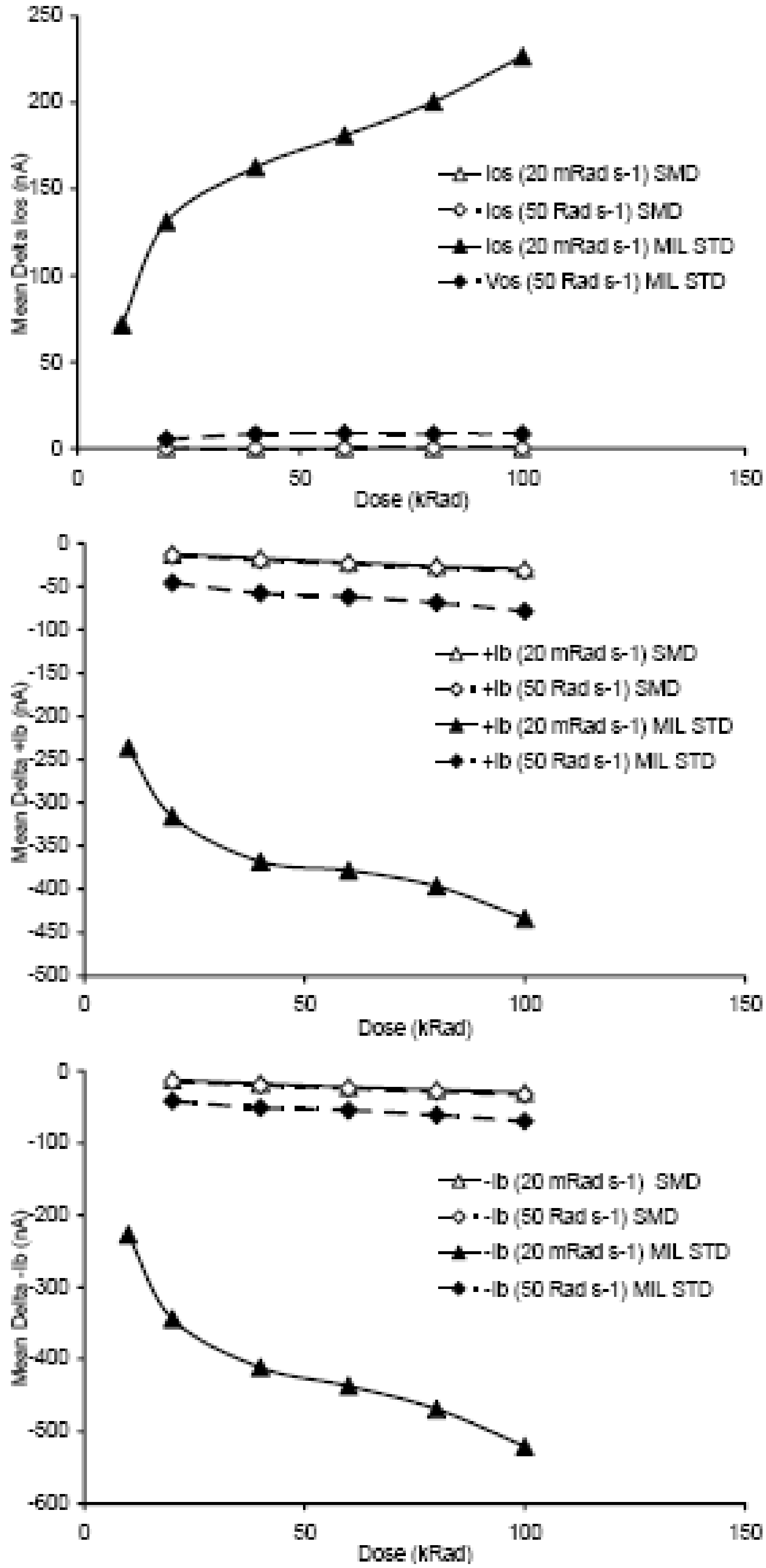

Figure 27. Dose rate dependencies for several parameters of SMD and MIL-STD screened (Ref 5).

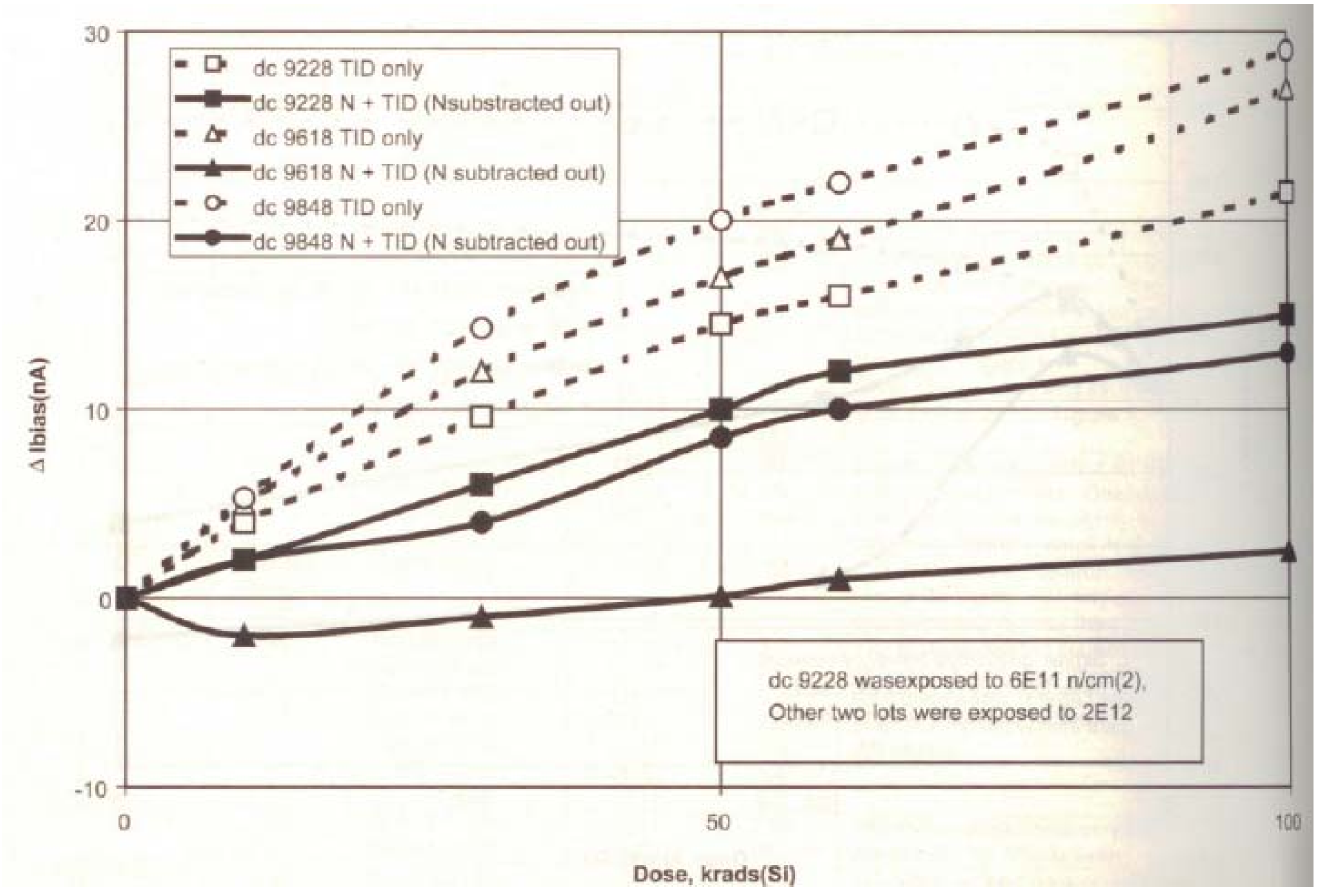

Figure 28. LM 124 neutron irradiated devices exhibit decreased gamma sensitivity compared to devices that were only total dose exposed. (Ref. 6)

The LM124 was quite sensitive to neutron fluence. The curves show that parts exposed to neutrons degraded less with total dose than those only total dose exposed. The curve doesn't show how much neutron degradation there was but Table 1 of Ref 6 does. IB degraded to 86 nA at 6E11 n/cm2. Figure 28 shows IB degradation between 21 – 29 nA at 100 kRad.

REF02AZ/QMLR (5962R8551401VPA):

The REF02AZ voltage reference is manufactured by Analog Devices, Inc. This new SMD version is guaranteed to 100 kRad. These parts are not dose rate sensitive (Ref 7).

Pre and post 100 kRad irradiation limits are identical to those listed in the part's specifications under AC and DC electrical characteristics as shown in Table 5 for 100 kRad.

Neutron degradation at 2E12 is small compared to TID at 100k. One can ignore neutron effects on this part (Ref 7).

Table 5. Electrical characteristics. Limits are post 100kRad irradiation.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Quiescent supply current	I_{SY}	No load	1	All		1.4	mA
			2,3			2.0	
		M,D,P,L,R 2/ 3/	1	01		1.4	
Output adjustment 4/ range	ΔV_{TRIM}	R_P = 10 kΩ, T_A = +25°C	1	All	±3.0		%
Output voltage	V_O	I_L = 0 mA	1	01,03	4.985	5.015	V
				02,04	4.975	5.025	
			2,3	01,03	4.978	5.022	
				02,04	4.953	5.047	
		M,D,P,L,R 2/ 3/	1	01	4.975	5.025	
Short circuit current 4/	I_{OS}	V_O = 0 V, T_A = +25°C	1	All	+15	+60	mA
Sink current 4/	I_S	T_A = +25°C	1	All	-0.3		mA
Load regulation	LD reg	I_L = 0 mA to 10 mA 5/	1	All		0.01	%/mA
		M,D,P,L,R 2/ 3/	1	01		0.015	
		I_L = 0 mA to 8 mA 5/	2,3	01,03		0.012	
				02,04		0.015	
Line regulation	LN reg	V_{IN} = 8 V to 33 V 5/	1	01,03		0.010	%/V
				02,04		0.012	
			2,3	All		0.015	
		M,D,P,L,R 2/ 3/	1	01		0.030	
Load current	I_L	T_A = +25°C 4/ 6/	1	All	10		mA
Output voltage noise	enp-p	0.1 Hz to 10 Hz 4/	4	01,02		18	μVP-P
				03,04		100	
Output voltage temperature coefficient	TCV_O	4/ 7/	8	01,03		±8.5	ppm/°C
				02,04		±25	

1/ V_{IN} = 15 V.
2/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
3/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
4/ This parameter is not tested to post irradiation.
5/ Line and load regulation specifications include the effect of self heating.

LP2953AMWG-QMLV (5962-9233601QXA):

The LP2953 is 16 pin ceramic surface mount adjustable voltage regulator manufactured by National Semiconductor ("National").

The LP2953 SMD version is very soft to total dose effect. Several sources of data including National website show similar results. In Ref 8, after the first irradiation step of 2.5 kRad, electrical parameters start to degrade, and one part out of 4 is out of specification limits. All parts are significantly degraded after the 30 kRad irradiation step. In addition, the part exhibits ELDRS effects; it is quite soft, 10-20 kRads at best (Ref 9).

Figure 29 shows the output short circuit current degradation for two date codes. Irradiation dose rate was 0.005 rad/sec. In an actual application, the output stage can no longer support the output load and the output will fall to zero and is considered failure under such load conditions. It is shown that lot to lot variability is large. The spec limit is exceeded at 4kRad in one date code, which is an extremely low failure level.

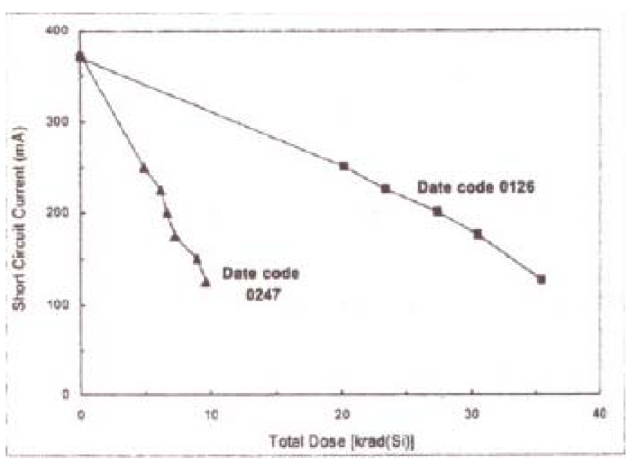

Figure 29. Short circuit current degradation for the 5962-9233601QXA version

Recently, National made some changes to this part and/or its die and the part became softer. This is a common theme and problem amongst analog IC manufacturers. Also, National's website has some data on their product lines. Figures 30-32, below, represents the older technology, suggest this part is functional to 50kRad. That is no longer true. Low dose rate testing, however, show most parameters to fail between 10 and 50 kRad. High dose rate test results show that all parameters meet the manufacturer's specification beyond 100 kRad(Si). Maximum output current, Fig. 30, degrades to an unusable level at about 50 kRad for the unbiased condition. The high rate condition had very little degradation and no bias effect whatsoever. In contrast, the low dose rate case had a significant bias effect. Shown in Fig. 31, the output voltage degraded very little for the high rate condition while at the low rate parts began to fail the specification limit below 20 kRad. The reference voltage degrades similarly indicating that reference voltage shift is primarily responsible for output voltage change. Unlike the other parameters, the dropout voltage degrades most for the 'biased' low dose rate case as shown in Fig. 32.

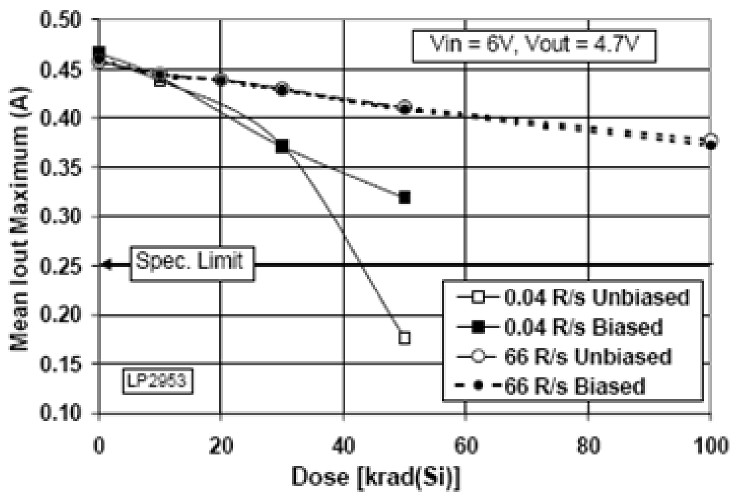

Figure 30. Maximum output current for LP2953 degrades more for the unbiased low rate case. No effect seen for the high dose rate case

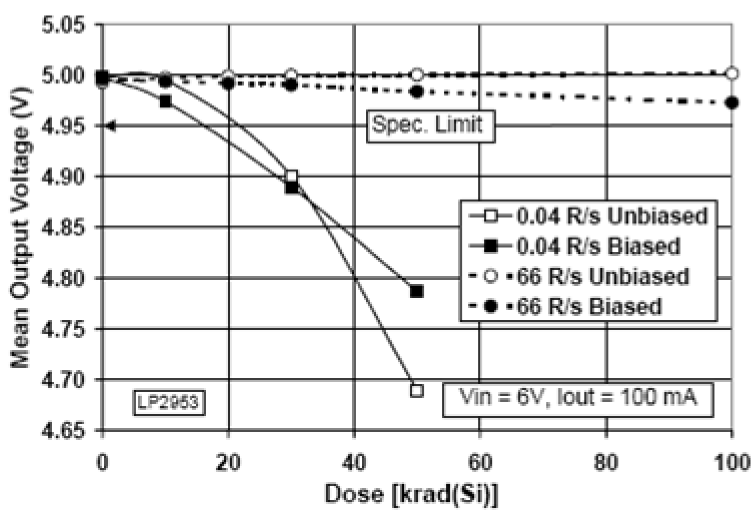

Figure 31, Output voltage degrade rapidly at low dose rate while little degradation is seen for the high dose rate case.

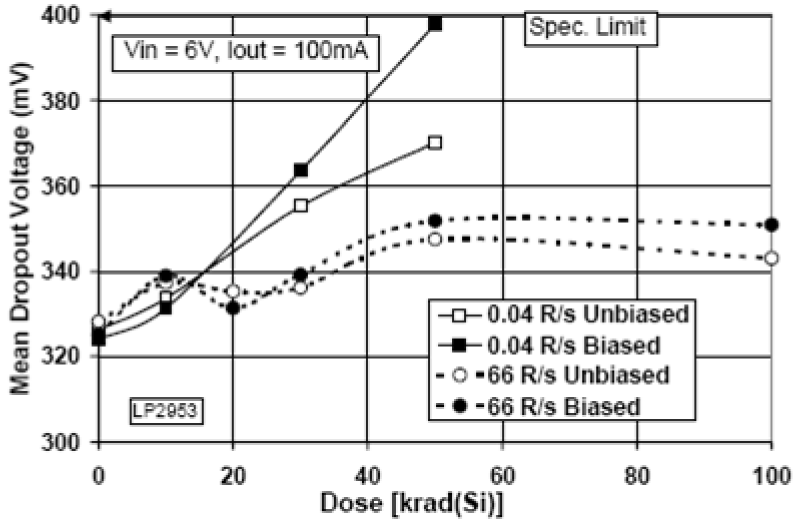

Figure 32, Dropout voltage degrades more for the biased low dose rate condition than the unbiased condition.

Displacement damage is shown in Figure 9 for 51 MeV proton irradiation. At this energy, the proton fluence of 1E11 p/cm2 is equivalent to ~ 2.5E11 n/cm2. The short circuit current degraded to 200 mA at this fluence. The pre irradiation spec limit is 500 mA.

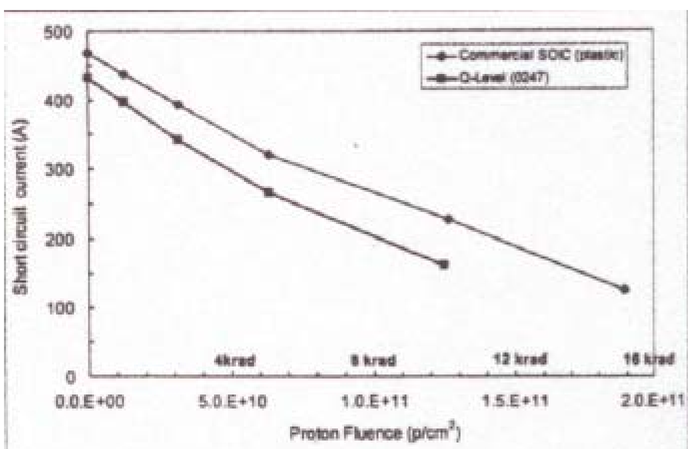

Figure 33 Short circuit current degradation with 51 MeV proton irradiation of 5962-9233601QXA version.

53124-110:

The 53124 is the Radiation Tolerant version of the standard 53111— 90V/ 1.6A (DC). It has several slight parametric differences from the 53111, but was designed for replacing the standard device when higher radiation tolerance is required. This design performs acceptably up to 300 kRads(Si) Total Dose. NASA has evaluated the electrical performance data of the 53124 against its competition in a particular application and reported superior results. See NASA report comparing 53124 to HSSR-7111. (Ref 10). All parameters tested remained well within the specifications to 100 kRad(Si).

The output leakage, however, does show more shift, a 15X increase (Figure 34), but it remains within the spec limit of 10 uA. The other parameters do not show any significant degradation as shown in Table 6.

Table 6 shows the degradation of the 53124 with total dose (Ref 1). 3 samples were tested

Total Dose in rad(Si)	T_{ON} (ms)	T_R (ms)	T_{OFF} (μs)	R_{ON} (connection A) (Ω)	R_{ON} (connection B) (Ω)	I_{OFF} (nA)	V_F (V)	V_R (V)
0	2.11	0.90	69	0.756	0.189	0.14	1.360	30.9
25k				0.752	0.188	0.95	1.360	31.3
50k	2.25	1.05	69	0.747	0.187	1.77	1.362	31.4
75k				0.753	0.188	2.68	1.362	30.9
100k	2.24	1.05	69	0.757	0.189	3.41	1.362	31.0

Average Post-irradiation Data for 53246 Solid State Relay

Total Dose in rad(Si)	T_{ON} (ms)	T_R (ms)	T_{OFF} (ms)	T_F (ms)	R_{ON} (mΩ)	I_{OFF} (nA)	V_F (V)	V_R (V)
0	3.32	2.65	55.2	28.0	29	0.8	3.731	45.5
25k					31	16.3	3.723	45.6
50k	2.98	2.32	59.0	29.0	29	27.6	3.735	45.4
75k					30	49.5	3.725	45.5
100k	3.65	2.73	60.3	30.3	30	60.1	3.729	45.5

Average Post-irradiation Data for 53250 Solid State Relay

Total Dose in rad(Si)	T_{ON} (ms)	T_R (ms)	T_{OFF} (ms)	T_F (ms)	R_{ON} (mΩ)	I_{OFF} (nA)	V_F (V)	V_R (V)
0	2.90	2.20	0.36	0.19	30	0.6	3.774	48.9
25k					30	14.6	3.771	49.0
50k	2.80	2.06	0.46	0.24	30	26.1	3.776	49.6
75k					30	40.5	3.774	49.7
100k	2.84	2.18	0.63	0.35	31	56.4	3.775	50.0

T_{ON} : turn-on time from 50% of input to 90% of output load;
T_R : load-current rise time from 10 to 90%;
T_{OFF} : turn-off time from 50% of input to 10% of output load;
T_F : load-current fall time from 90 to 10%;
R_{ON} : on-state output resistance;
I_{OFF} : off-state output (leakage)current;
V_F : forward bias voltage of the input LED;
V_R : reverse breakdown voltage of the input LED.

Parameter Symbols for operational amplifier

V_{OS} : input offset voltage;
I_{IN} : input bias current;
I_{OS} : input bias current offset;
A_{VOL} : open loop voltage gain;
I_{CC} : positive supply current.

Output Leakage Current (connection A) vs Total Dose

Test conditions: V_f = 1.0V, V(out) = 90V						
Date	Total Dose (krad(Si))	1	2	4	5	7*
		(nA)				
8/16	0	0.20	0.13	0.15	0.11	0.14
8/17	25	1.00	0.89	0.94	0.96	0.13
8/18	50	1.89	1.68	1.74	1.75	0.13
8/18	75	2.82	2.54	2.60	2.77	0.14
8/18	100	3.58	3.20	3.28	3.57	0.14

* indicates control unit

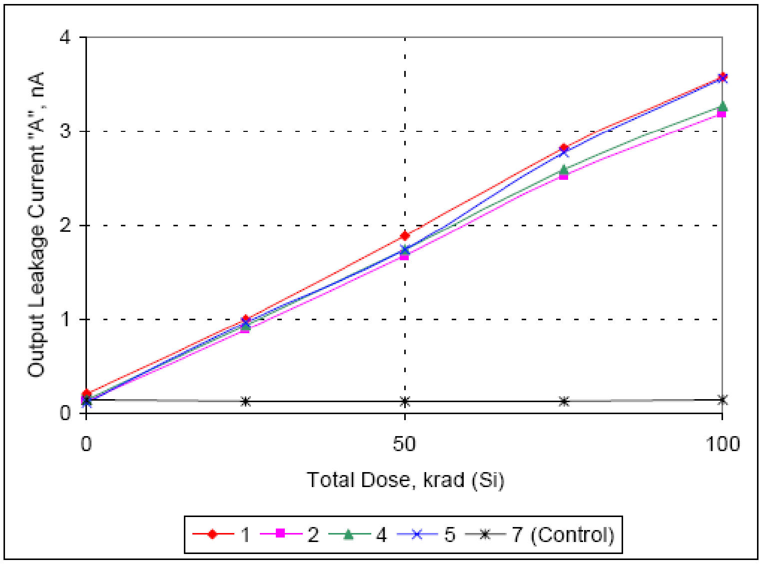

Figure 34. Output Leakage show increased leakage

The part was tested with protons (Ref. 11). There was a nominal increase in the forward current threshold for the LED but the threshold remained below the minimum specification limit for operating the devices. There was also no pronounced change in the output currents of the devices. Each DUT was tested to a total fluence of 1x1012 p/cm^2. This is equivalent to ~ 2.5E12 neutrons/cm^2.

53111-110:

Micropac 53111 is a one-channel power MOSFET opto-coupler hermetically sealed with an 8-pin ceramic DIP package. This is 90 V/ 1.6A (DC), .8A AC/DC SSR or Power MOSFET opto-coupler.

This product was not designed to be a Radiation Tolerant Product but did pass after 60 kRads (Si) total dose (Ref 12). The parameters measured remained within specification after receiving a total dose of 60 kRads (Si) at a dose rate of 2.5 kRad/min. Small increases in Von and toff were observed, as well as small decreases in Vf. Other parameters did not change outside of the experimental error (Table 7). The tables show that the part exhibits little to no change out to 100 kRads. All parameters remained within spec limits.

Table 7. Pre and Post Irradiation data on one sample showing insignificant degradation

UNIT NO. 5 (CONTROL UNIT)

Total Dose (Kradsi)	V_f (volt)	V_{on} (milli-volt)	V_L (micro-volt)	V_R (volt)	t_{on} (milli-sec)	t_{off} (micro-sec)
0	1.262	15.96	100?	35.6	1.702	122
0	1.263	15.9	100?	35.6	1.602	123
0	1.262	16	0	35.6	1.682	125
0	1.262	16	0	35.6	1.63	126
0	1.261	16	0	35.6	1.655	124
0	1.262	16	0	35.6	1.625	126
0	1.261	16	0	35.6	1.67	125
0	1.261	16	0	35.6	1.595	126
0	1.26	16	0	35.6	1.65	125
0	1.261	16	0	35.6	1.64	125
0	1.26	16.1	0	35.7	1.64	125

Total Dose (Kradsi)	V_f (volt)	V_{on} (milli-volt)	V_L (micro-volt)	V_R (volt)	t_{on} (milli-sec)	t_{off} (micro-sec)
0	1.26	16.1	100?	31.8	2.2	77
15	1.256	16.4	90?	32.3	2.195	79
20	1.256	16.4	0	30.2	2.18	79
25	1.257	16.2	0	30.5	2.205	79
30	1.256	16.3	10	30.5	2.16	79
35	1.256	16.3	10	30.7	2.165	81
40	1.256	16.4	10	30.9	2.115	80
45	1.255	16.3	10	30.9	2.165	80
50	1.254	16.4	10	31.1	2.195	80
55	1.256	16.4	10	30.9	2.17	80
60	1.255	16.4	10	30.9	2.265	81

Power MOSFET opto-couplers were exposed to 14 MeV neutrons and Co-60 gammas. Radiation from neutron activation of the package materials had a significant effect on the electrical parameters of the devices. (Ref. 13).

3.0 CONCLUSIONS AND RECOMMENDATIONS

In the SET analysis, each component was first analyzed individually to determine the SET levels. These upsets were then simulated at the circuit level to determine the effect on the performance of the circuit function. The simulations are heavily reliant on the SPICE models of the individual devices, which we assume to be valid for the recovery of the transient event. Subsequent bench testing should be used to confirm the performance expectations. In the end result, none of the event transient altered the state of the over-voltage function, so that there are zero upsets and the SET requirement of < 1E-3 per year is met.

The SEU, SEL, SEG, and SEGR requirements are also met.

The TID/DD requirements call for a 2x design margin. However, very little performance data is available at 200kRad for most of the integrated circuits. Therefore, their degradation beyond the 100kRad results reported is unknown.

Worst case circuit analysis should be done to compute an end-of-life value for all critical circuit performance characteristics. This data would be put into a worst case circuit analysis to confirm that the end-of-life performance is acceptable. For parameter P one would have Peol = Pspec limit + DP(temp) + DP(aging) + DP(dose) + DP(displacement). The dose and displacement levels would have to be at least 2X of the predicted values. If the degradation at the levels with 100 mils is excessive, then additional shielding will be required. Since dose and displacement occur concurrently, one cannot separate the two. Shielding will reduce both levels and both shifts.

The LP2953 and the 53111 failed at low TID levels of 30 and 60 kRad. All other parts passed at 100 kRad.

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