AEi Systems

Power IC Model Library™

for PSpice®

Model Documentation

Version 4.5, 2024

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Chapter 1 - Overview

Welcome

Thank you for purchasing the AEi Systems Power IC Model Library for PSpice.

SMPS applications today are much more demanding than ever. Today's designs require increases in switching frequency, higher efficiency, and lower standby current. State space based models simply do not reveal many important nonlinear factors that influence these performance characteristics. To address the needs of today's power supply designer, AEi Systems introduced the Power IC Model Library for PSpice. This library represents a breakthrough for SMPS designers who use PSpice.

AEi Systems has spent years developing accurate and robust models for the components that are used in power designs. We test our models thoroughly so you can have confidence in the model's operation and results. Useful examples are also provided for most of the models.

The library incorporates a comprehensive set of large signal hyper-accurate cycle-by-cycle simulation models for Pulse Width Modulation (PWM), Switching Regulators, Phase Shift Controllers, and other Power ICs. You can perform high-speed, cycle-by-cycle simulation to show true large-signal performance, simulate current-mode control using the latest accurate modeling techniques, run CCM and DCM converter simulations, analyze control systems including loop gain, input filter design and analysis, and measure power stage loss and stress analysis for all major components. In summary, you can simulate your entire power system.

Nonlinear characteristics such as propagation delay, switching speed, drive capability and maximum duty cycle/current limits, startup phenomena are all accurately modeled. You can directly compare the performance of components from different vendors and analyze the effects of different implementations such as peak current mode control, hysteretic current control, low voltage, and low operating current, to name just a few.

Summary of Benefits:

- Analyze large signal effects like start-up transients, power stage semiconductor stress, and step-load response
- Explore different approaches to transformer, converter, filter, and control structures
- Compute component stresses and test for excessive power dissipation
- Compare circuit characteristics with linear and nonlinear magnetics
- Analyze in both time and frequency domains
- Simulate and analyze your entire power supply without ANY limitations.

The models utilize analog behavioral elements, special Boolean logic elements and other

specially designed function blocks. Together they greatly reduce the model's simulation runtime, while maintaining "better than data sheet max/min" accuracy, an important factor in SMPS analysis.

Components are normally modeled to match "Typical" part performance at room temperature. Some temperature performance variations are also taken into account.

What's Included – Getting Started

The Power IC Model Library includes over 1,700 PSpice syntax compatible models in multiple model library files (See Chapter 4, Library Listings). Example schematics in native format and symbols for both OrCAD Capture and MicroSim Schematics are included.

Files included and their location after installation:

EMA\PowerIC_Library Folder - License files and documentation

Library Folder - Models and Symbols

- PSpice Model Libraries Files for both Capture and Schematics (.LIB)
- Symbol Files for both Capture and Schematics (.OLB, .OLJ, .SLB)

Examples Folder – OrCAD Capture Schematics

Various Folders (by manufacturer)

- Capture schematic files (.OPJ, .DSN, .SCH)

MicroSim Folder - MicroSim Schematics Files

Various Folders (by manufacturer)

- Schematics Files (.SCH, .NET, .ALS, etc.)

Documentation Folder - Manual and Model Reference Documentation

Installing Schematic, Library, or Symbol Files

The Power IC Model Library installation utility will install the library and other files onto your computer regardless of the version of PSpice you are using.

The Power IC Model library will need to be configured manually in OrCAD to use the libraries. Please follow the instructions provided in the next section. Please see the relevant portions of your OrCAD or MicroSim User's Guide for details on how to incorporate new models and/or symbols into the design environment.

Symbol and model libraries generally use the name of the IC manufacturer whose parts are modeled in the library. The models in a .LIB file have corresponding symbols in the same named symbol file. Please see Chapter 4, Library Listings, for information on where specific models and symbols are located.

Master Library File

The **Power_EMA_AEI.LIB** file contains a list of all the library files and may be used to include all the models in the Power IC Model Libraries in a manner like the NOM.LIB file (Nom.Lib is distributed with PSpice).

In some cases, common sub-blocks called by a subcircuit in one library might be located in another library. That's why it is best to use the Power_EMA_AEI.LIB master library file to incorporate models into your simulations and schematic environment.

Important Note: It is recommended that Power IC Model Library files and symbols NOT be placed in the same directory as the OrCAD delivered files in order to avoid any naming conflicts that may arise in the future.

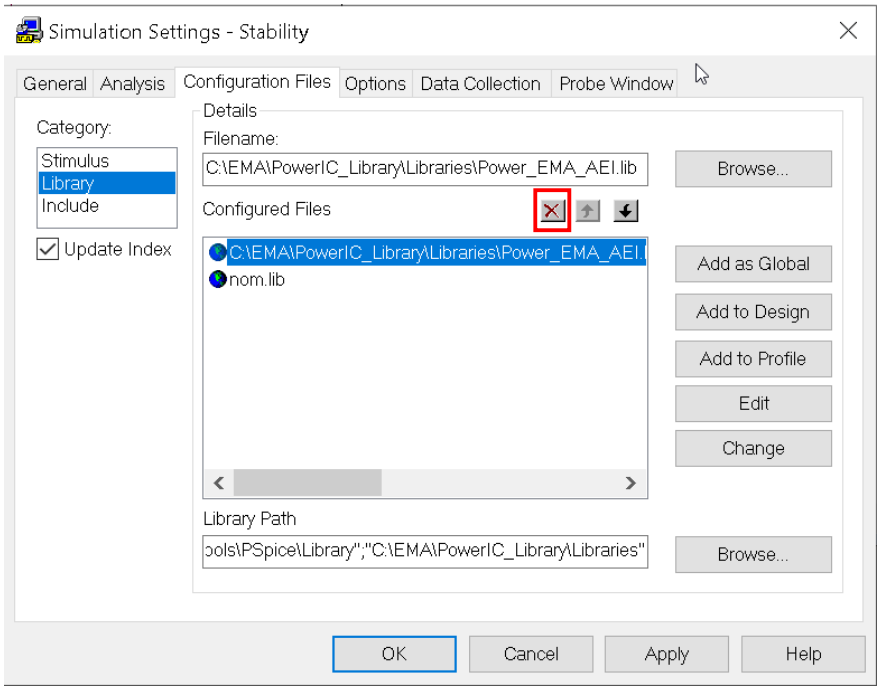
MicroSim Schematics

While the MicroSim Schematics files are included in the relevant OrCAD schematics folders a separate folder set is included for MicroSim Schematics users that only includes the relevant *.SCH file, without any OrCAD Capture related files.

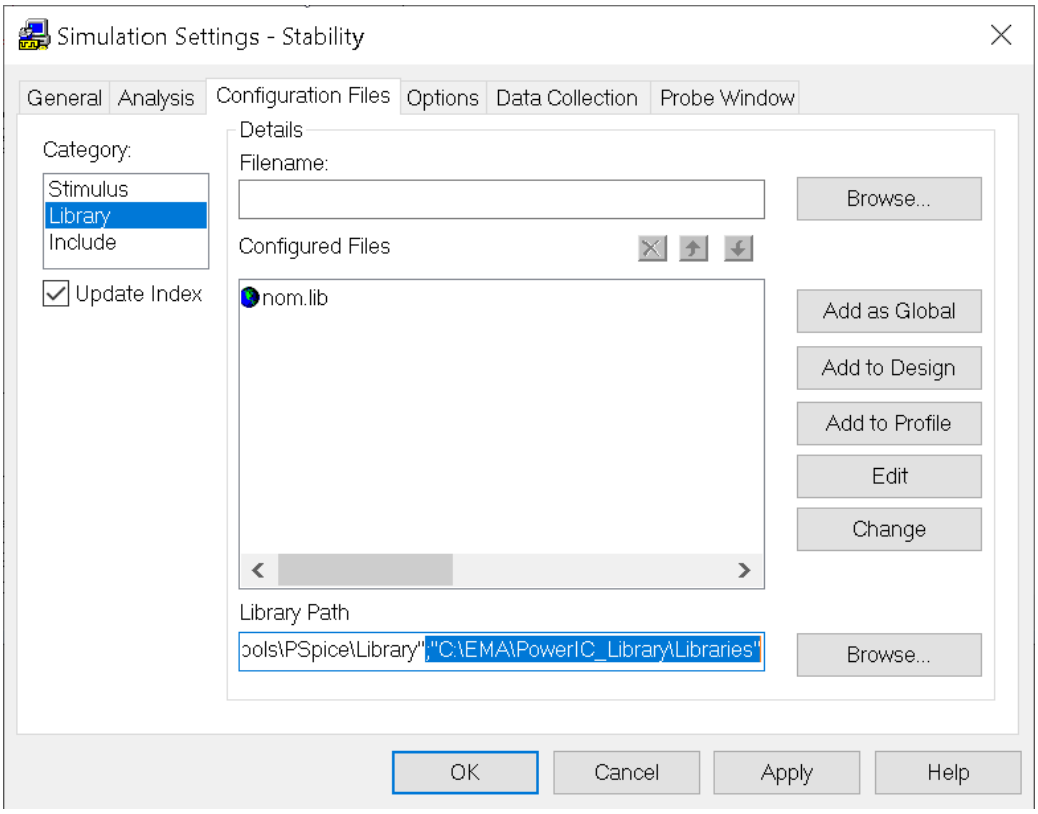
You may have to edit the Library Settings using the Editor Configuration function in the Options menu in order to get MicroSim Schematics to recognize the .SLB symbol files.

Uninstalling the Power Library Files

1. Use the Add/Remove Program feature in the Window Control Panel to uninstall the Power IC Model Library.
2. After the uninstalling is complete, go to the Simulation Settings window and select the Power IC Model Libraries from the list in the Configured Files section.
3. Delete the Power_EMA_AEI.lib item from this list, by clicking on the "X" symbol button just above the list.



4. Delete the portion of the Library Path where the Power IC Model Libraries was installed (including the semicolon). By default, this is ";C:\EMA\PowerIC_Library\Libraries"

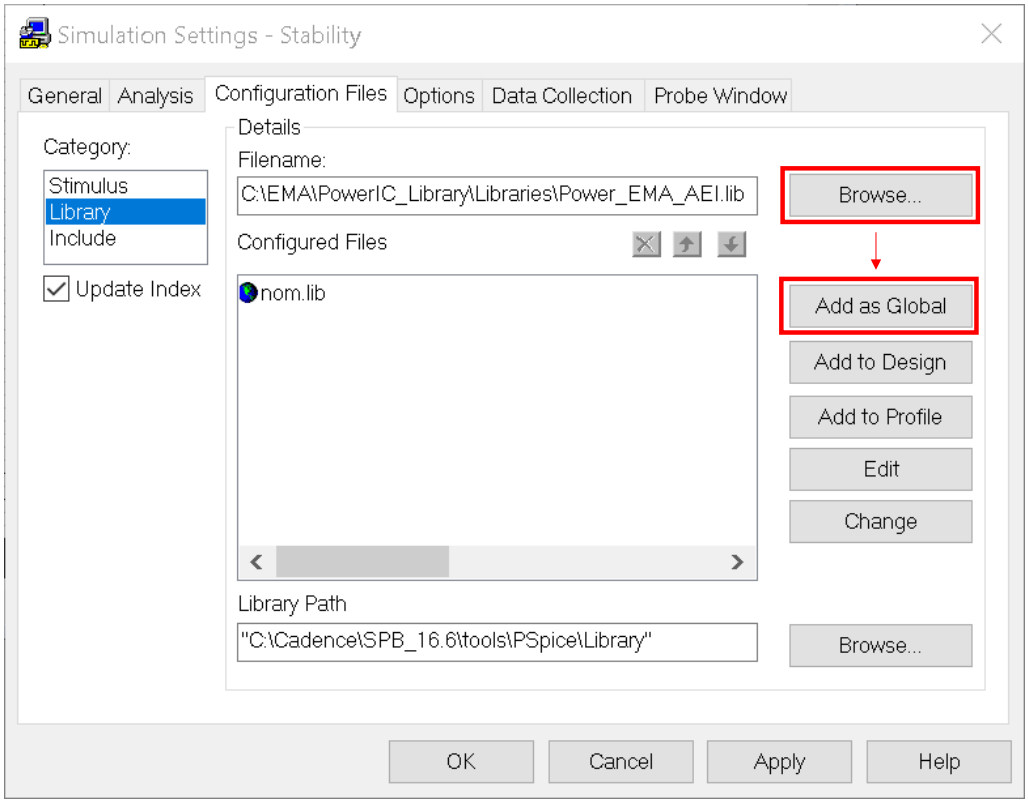


5. This will ensure that Power IC Model Library and its components are completely removed from all your future PSpice projects.

Configuring the Power Library

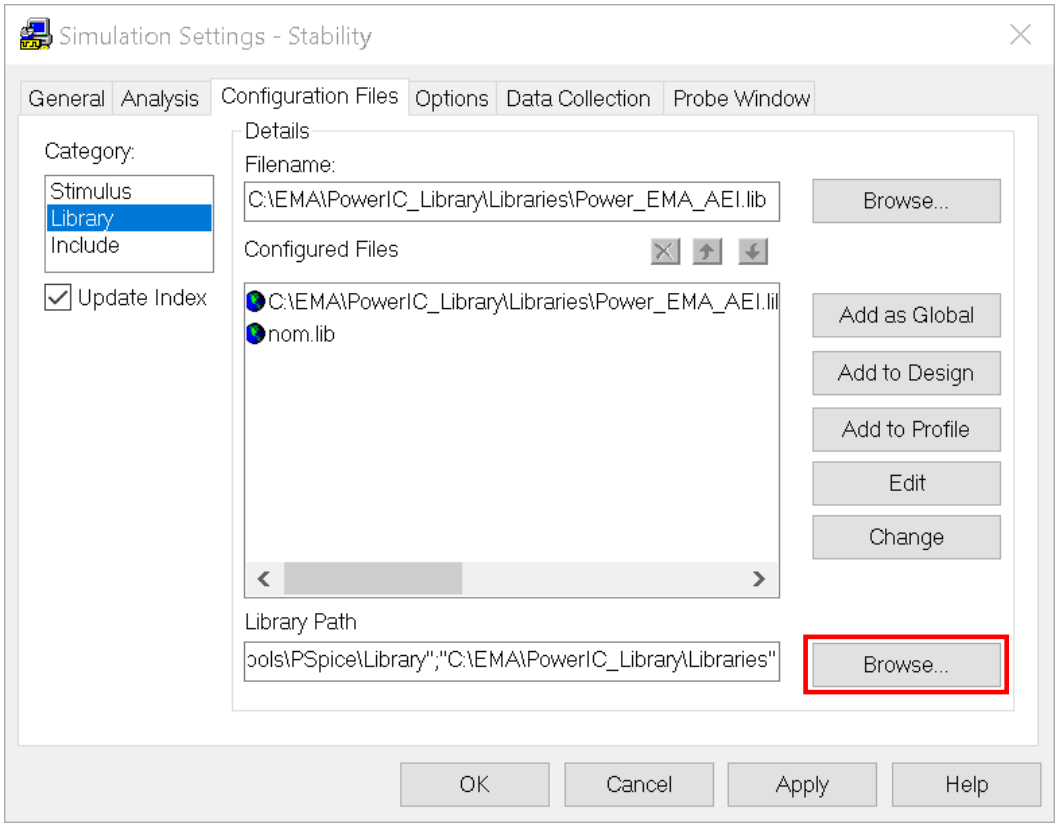
1. Open a new or an existing PSpice project.
2. From the PSpice Menu, choose New Simulation Profile (provide a new name for the profile) or Edit Simulation Profile.
3. In the Simulation Settings window, chose the Configuration Files tab.
4. Choose Library from the Category list, seen on the left-hand side.
5. Click on the Browse button in the Details section to the right of the Filename box and browse to the location in your machine where the Power IC Model Library was installed during the installation process. By default, the library and its components are saved within **C:\EMA\PowerIC_Library.**
6. Locate "Power_EMA_AEI.lib" which is in C:\EMA\PowerIC_Library\Libraries and click Open.

7. Click on Add as Global and the models in the Power IC Model Libraries (which now will appear on the top of the list under Configured Files section) are now ready to use in your PSpice projects.



Optional: To be able to right click on a symbol of a model from the Power IC Model Library and select Edit PSpice Model, you need to perform this step.

8. Click on the Browse button in the Details section to the right of the Library Path box and browse to the library path of where the Power IC Model Library was installed during the installation process and click on the OK button. The file path will be appended onto the Library Path string by a semicolon (;). By default, the library files are saved within C:\EMA\PowerIC_Library\Libraries



9. Click OK to exit the Simulation Settings window.

Model Documentation and Support

Each model in the AEi Systems Power IC library is tested under various conditions using multiple test circuits for specific functions and then again in one or more full application test circuits. The results are compared to data sheet performance and in most cases actual bench measurements.

AEi Systems strives to produce models that meet all key performance metrics and exhibit "typical" performance as specified in the data sheet or performance that is within given Max-Min specifications.

Adobe Acrobat .PDF files containing documentation for various models in the library are included in the Documentation folder on the distribution CD.

The documentation discusses the model development and architecture and contains the results of the testing and verification process.

The support section of AEi System's web site, http://www.aeng.com/support.htm, contains additional model documentation and various white papers on simulation and modeling.

Documentation for other models that are not on the distribution CD may or may not be available. Please inquire with AEi Systems directly at info@aeng.com.

If you purchased this library from EMA Design Automation, you may get support in any of the following ways:

EMA Resource Center	http://support.ema-eda.com
e-mail	techsupport@ema-eda.com
Telephone	585-334-6001 option 5

Chapter 2 - Model Discussions

Model Usage

Most of the models in the Power IC Model Libraries are transient time-domain models. That includes the FET Drivers and majority of the controller models (parts without an "s" extension in the model's name).

The controller models are normally pin-for-pin compatible with the actual physical part. All key functions of the actual chip are modeled except for variations with temperature. This includes startup nonlinearities and other transient phenomenon. Smoke alarm parameters are

not currently implemented. While over-current and other protection functions are modeled, stimulus or supply voltages that exceed the data sheet minimums or maximums may produce unreliable results.

The models are characterized for typical operation at room temperature.

The transient models can be used in all types of simulations including startup, line transient, load transient, and steady state, provided that the external circuit and stimulus are properly adjusted.

The transformer and semiconductor models can be used in either transient or frequency domain simulations.

For switching circuit simulations linearized models are required to perform frequency domain simulations. The switching based transient controller models cannot be used in frequency domain simulations. Models that are linearized fall into the classification of "state space" models. While a variety of state space models are available on the Internet, the Power IC Model Library includes Boost, Buck, Forward, and Flyback "PWM" blocks. See references 1 and 2 for more information on these blocks.

Frequency domain versions of various PWM controllers are included in the Power IC Model Library. Many will have an "s" appended to their model's name as in the LT1242s and UC1845As. Several example .AC simulations are included (UC1842STATESPACE.DSN, UC1843ASTEST.DSN, NCP1000AVGTEST.DSN, etc.). Please see the list of models, "Power_Library_List_4.4.pdf" for specific model names and functionality.

Using the Models with Other Simulators

To produce models that are accurate but run in a reasonable time frame, AEi Systems uses a combination of actual semiconductors and behavioral modeling constructs to model power ICs. Two constructs are utilized frequently: the switch with hysteresis and If-Then-Else expressions.

Not all versions of PSpice support a switch with hysteresis. While the S_ST Short-Transition switch model, which emulates the Berkeley SPICE 3 S element, is now available, older versions of PSpice (prior to v9.2.3) did not support the hysteresis effect. A subcircuit, shown below, is utilized in order to provide compatibility with all versions of PSpice without compromising performance.

```
.subckt SWhyste NodeMinus NodePlus Plus Minus PARAMS: RON=1 ROFF=100MEG
VT=1.5 VH=.5
S5 NodePlus NodeMinus 8 0 smoothSW
```

```
EBcrtl 8 0 Value = { IF ( V(plus)-V(minus) > V(ref), 1, 0 ) }
EBref ref1 0 Value = { IF ( V(8) > 0.5, {VT-VH}, {VT+VH} ) }
Rdel ref1 ref 70
Cdel ref 0 100p  IC={VT+VH}
Rconv1 8 0 10Meg
Rconv2 plus 0 10Meg
Rconv3 minus 0 10Meg
.model smoothSW VSWITCH (RON={RON} ROFF={ROFF} VON=1 VOFF=0)
.ends SWhyste
```

If-Then-Else expressions in the E and G elements are also used for various logic and controlling functions. In them, mathematical equations using Boolean combinations of node voltages and branch currents are utilized.

For example,

```
GB1 33 2 Value= { IF ( V(5) > 2.5 & V(11) > 4.3 , -.014 , 0 ) }
EB19 44 0 Value= { IF ( V(22)<1 , 2 , IF ( V(30)<1 & V(42)<1 , 2 , V(30) ) ) }
```

If you are trying to use the models with other SPICE based simulators you will have to make sure that the simulator supports these extensions to the basic SPICE primitive set.

If you need one or more of the models translated to another SPICE syntax, please contact AEi Systems directly.

Chapter 3 - Using the Power IC Model Schematic Examples

Schematic Examples

The Power IC Model Library for PSpice includes several application test circuit examples. Some are simple; others are complicated and mimic the actual applications circuit found in the data sheet. All should run in a few minutes or less on most computers.

The example schematic designs can be found in two folders on the distribution CD. Under the PowerIC_Library folder is an Examples folder. That contains the schematics for the OrCAD Capture system. The MicroSim folder contains approximately the same set of examples for the MicroSim Schematics environment.

A master library file has been created called Power_EMA_AEI.lib. It is in the Libraries folder along with the rest of the model libraries. You can refer to this file to include all of the models in the parts database for either OrCAD Capture Library Configuration or the MicroSim Schematics Library and Include Files… function (Analysis menu)

The MicroSim Schematics editor may not be able to find the symbol library files depending on where you choose to install them. You can correct this problem by pointing to the symbol library file on your hard disk using the Editor Configuration… function in the Options menu.
Most parts have an equivalent test circuit matched to their name. In some cases, where there is a family of parts there may be fewer test circuits than parts, but the parts are normally interchangeable, in so far as the test circuit is concerned, allowing the same test circuit to serve the part family.

The test circuits will allow you to explore the basic functionality of the model, if not its entire range of features.

Types of Simulations

Simulation Run Times
The time it takes to run a switch mode power supply simulation is directly related to a number of factors:

- Your computer's performance
- Complexity of the model and external circuitry
- Length of the simulation

- Time step of the simulator

The last item is driven by a number of factors including the stimulus and loading, soft-start and compensation components, the simulator .OPTION tolerances, the TMAX timestep setting, and the overall frequency content of the circuit (edge speeds).

It is not uncommon for SMPS simulations to take 15-60 minutes each. However, most of the example simulations run in just a few minutes.

Startup Simulations
Startup simulations can take a long time to run depending on the conditions and compensation settings. You can recognize these simulations in the examples because they normally don't use the UIC (use initial conditions) transient directive and use VCC/stimulus settings that start at zero and are pulsed on to their terminal voltage. In addition, initial conditions on input, output or compensation capacitors are not utilized.

Steady State, Line, Load Transient Simulations
In order to speed up the simulation of these types of analyses it is best to try to set initial conditions on key storage elements. This helps to get the circuit running at or near steady state almost immediately. This is as opposed to running a startup type simulation and delaying the data taking interval until steady state is achieved. To do this, the UIC option is used and IC= directives are inserted, especially on input output, and compensation capacitors.

Correct initial conditions can allow a circuit that would normally take several milliseconds of time to start to get to steady state in a few hundred microseconds.
Incorrect initial conditions, whether they are set by the .NODESET, .IC, or IC= directives can cause the PSpice simulation to take much longer than if it were started from a zero voltage state due to transient residues or can cause convergence problems. In some circuits the initial conditions on compensation components can be very sensitive with respect to simulation settling time, with a few tenths of a volt making a huge difference in settling/runtime.

Except in cases where the compensation is internal, the models in the Power IC Model Library are setup to allow you to achieve steady state by setting initial conditions on elements external to the part.

Simulation Convergence – Quick Fix

If you encounter a convergence problem, change the .OPTIONS settings you are using to the following:

- **Abstol = 0.01u (Default=1p)**

- **Vntol = 10u (Default=1u)**
- **Gmin=0.1n (Default=1p)**
- **Reltol = 0.01 (Default=0.001)**
- **ITL4 = 500 (Default=10)**

This should cure most simulation convergence problems unless there is an error in your circuit description.

Switching simulations refer to simulations which have a significant number of repetitive cycles, such as those found in SMPS simulations. Most of the simulations you perform with the Power IC Models will be of this type.

SMPS simulations can experience a large number of rejected time points. Rejected time points are due to the fact that PSpice has a dynamically varying time step which is controlled by constant tolerance values (Reltol, Abstol, Vntol). An event that occurs during each cycle, such as the switching of a power semiconductor, can trigger a reduction in the time step value. This is caused by the fact that PSpice attempts to maintain a specific accuracy and adjusts the time step in order to accomplish this task. The time step is increased after the event, until the next cycle, when it is again reduced. This time step hysteresis can cause an excessive number of unnecessary calculations. To correct this problem, we can regress to a SPICE 2 methodology and force the simulator to have a fixed time step value.

To force the time step to be a fixed value, set the Trtol value to 25, i.e. .OPTIONS TRTOL=25. The default value is 7. The Trtol parameter controls how far ahead in time SPICE tries to jump. The value of 25 causes PSpice to try to jump far ahead. Then set the Tmax value (maximum allowed time step) in the .TRAN statement to a value which is between 1/10 and 1/100 of the switching cycle period. This has the opposite effect; it forces the time step to be limited. Together, they effectively lock the simulator time step to a value which is between 1/10 and 1/100 of the switching cycle period, and eliminate virtually all of the rejected time points. These settings can result in over a 100% increase in speed!

Note: In order to verify the number of accepted and rejected time points, you may issue the .OPTIONS ACCT parameter and view the data at the end of the output file.

If this does not help the simulation converge proceed to the next section which has more details.

Simulation Convergence

The answer to a nonlinear problem, such as those in the SPICE DC and Transient analyses, is found via an iterative solution. For example, PSpice makes an initial guess at the circuit's node voltages and then, using the circuit conductances, calculates the mesh currents. The

currents are then used to recalculate the node voltages, and the cycle begins again. This continues until all of the node voltages settle to values which are within specific tolerance limits. These limits can be altered using various .Options parameters such as Reltol, Vntol, and Abstol.

If the node voltages do not settle down within a certain number of iterations, the DC analysis will issue an error message such as "No convergence in DC analysis", "Singular Matrix", or "Source Stepping Failed". PSpice will then halt the run because both the AC and transient analyses require an initial stable operating point in order to proceed. During the transient analysis, this iterative process is repeated for each individual time step. If the node voltages do not settle down, the time step is reduced and PSpice tries again to determine the node voltages. If the time step is reduced beyond a specific fraction of the total analysis time, the transient analysis will issue the error message, "Time step too small," and the analysis will be halted.

Convergence problems come in all shapes, sizes, and disguises, but they are usually related to one of the following:

- Circuit Topology
- Device Modeling
- Simulator Setup

The DC analysis may fail to converge because of incorrect initial voltage estimates, model discontinuities, unstable/bistable operation, or unrealistic circuit impedances. Transient analysis failures are usually due to model discontinuities or unrealistic circuit, source, or parasitic modeling. In general, you will have problems if the impedances, or impedance changes, do not remain reasonable. Convergence problems will result if the impedances in your circuit are too high or too low.

The various solutions to convergence problems fall under one of two types. Some are simply band-aids which merely attempt to fix the symptom by adjusting the simulator options. Other solutions affect the true cause of the convergence problems.

The following techniques can be used to solve many convergence problems. When a convergence problem is encountered, you should start at solution 0 and proceed with the subsequent suggestions until convergence is achieved. The sequence of the suggestions is structured so that they can be incrementally added to the simulation. The sequence is also defined so that the initial suggestions will be of the most benefit. Note that suggestions which involve simulation options may simply mask the underlying circuit instabilities. Invariably, you will find that once the circuit is properly modeled, many of the "options" fixes will no longer be required!

General Discussion

Many power electronics convergence problems can be solved with the .OPTIONS Gmin parameter. Gmin is the minimum conductance across all semiconductor junctions. The conductance is used to keep the matrix well-conditioned. Its default value is 1E-12mhos. Setting Gmin to a value between 1n and 10n will often solve convergence problems. Setting Gmin to a value which is greater than 10n may cause convergence problems.

PSpice does not always converge when relaxed tolerances are used. One of the most common problems is the incorrect use of the .Options parameters. For example, setting the tolerance option, Reltol, to a value which is greater than .01 will often cause convergence problems.

Setting the value of Abstol to 1u will help in the case of circuits that have currents which are larger than several amps. Again, do not overdo this setting. Setting Abstol to a value which is greater than 1u may cause more convergence problems than it will solve.

After you've performed a number of simulations, you will discover the options which work best for your circuit. Very often various options will be needed as the circuit topology is developed. Invariably, you will find that after you have debugged your circuit representation, and if your components are well modeled, most of the options can be removed.

If all else fails, you can almost always get a circuit to simulate in a transient simulation if you begin with a zero voltage/zero current state. This makes sense if you consider the fact that the simulation always starts with the assumption that all voltages and currents are zero. The simulator can almost always track the nodes from a zero condition. Running the simulation will often help uncover the cause of the convergence failure.

The above recommendation is only true if your circuit is constructed properly. Most of the time, minor mistakes are the cause of convergence problems. Error messages will help you track down the problems, however, a good technique is to scan each line of the netlist and look for anomalies. It may be tedious, but it's a proven way to weed out mistakes.

Not all convergence failures are a result of the PSpice software! Convergence failures may identify many circuit problems. Check your circuits carefully, and don't be too quick to blame the software.

DC Convergence Solutions

0. Check the circuit topology and connectivity.

Common mistakes and problems:

- Make sure that all of the circuit connections are valid. Also, verify component polarity.
- Check for syntax mistakes. Make sure that you used the correct SPICE units (i.e. MEG instead of M(milli) for 1E6).
- Make sure that there is a DC path from every node to ground.
- Make sure that voltage/current generators use realistic values, especially for rise and fall time
- Make sure that dependent source gains are correct, and that E/G element expressions are reasonable. If you are using division in an expression, verify that division by zero cannot occur or protect against it with a small offset in the denominator.

1. **Increase ITL1 to 400 in the .OPTIONS statement.**
   Example: .OPTIONS ITL1=400

This increases the number of DC iterations that PSpice will perform before it gives up. In all but the most complex circuits, further increases in ITL1 won't typically aid convergence.

2. **Add .NODESETs**
   Example: .NODESET V(6)=0

View the node voltage/branch current table in the output file. PSpice produces one even if the circuit does not converge. Add .NODESET values for the top level circuit nodes (not the subcircuit nodes) that have unrealistic values. You do not need to nodeset every node. Use a .NODESET value of 0V if you do not have a better estimation of the proper DC voltage. Caution is warranted, however, for an inaccurate Nodeset value may cause undesirable results.

3. **Add resistors and use the OFF keyword.**
   Example: D1 1 2 DMOD OFF
   RD1 1 2 100MEG

Add resistors across diodes in order to simulate leakage. Add resistors across MOSFET drain-to-source connections to simulate realistic channel impedances. This will make the impedances reasonable so that they will be neither too high nor too low. Add ohmic resistances (RC, RB, RE) to transistors. Use the .Options statement to reduce Gmin by an order of magnitude.

Next, you can also add the OFF keyword to semiconductors (especially diodes) that may be causing convergence problems. The OFF keyword tells PSpice to first solve the operating point with the device turned off. Then the device is turned on, and the previous operating point is used as a starting condition for the final operating point calculation.

4. **Use PULSE statements to turn on DC power supplies.**
   Example: VCC 1 0 15 DC
   becomes VCC 1 0 PULSE 0 15

This allows the user to selectively turn on specific power supplies. This is sometimes known as the "Pseudo-Transient" start-up method. Use a reasonable rise time in the PULSE

statement to simulate realistic turn on. For example,

V1 1 0 PULSE 0 5 0 1U

will provide a 5 volt supply with a turn on time of 1μs. The first value after the 5 (in this case, 0) is the turn-on delay, which can be used to allow the circuit to stabilize before the power supply is applied.

5. Add UIC (Use Initial Conditions) to the .TRAN statement.

Example: .TRAN .1N 100N UIC

Insert the UIC keyword in the .TRAN statement. Use Initial Conditions (UIC) will cause PSpice to completely bypass the DC analysis. You should add any applicable .IC and IC= initial conditions statements to assist in the initial stages of the transient analysis. Be careful when you set initial conditions, for a poor setting may cause convergence difficulties.

AC Analysis Note: Solutions 4 and 5 should be used only as a last resort, because they will not produce a valid DC operating point for the circuit (all supplies may not be turned on and circuit may not be properly biased). Therefore, you cannot use solutions 4 and 5 if you want to perform an AC analysis, because the AC analysis must be preceded by a valid operating point solution. However, if your goal is to proceed to the transient analysis, then solutions 4 and 5 may help you and may possibly uncover the hidden problems which plague the DC analysis.

Transient Convergence Solutions

0. Check circuit topology and connectivity.

This item is the same as item 0 in the DC analysis.

1. Set RELTOL=0.01 or 0.005 in the .OPTIONS statement.

Example: .OPTIONS RELTOL=0.01

This option is encouraged for most simulations, since the reduction of Reltol can increase the simulation speed by 10 to 50%. Only a minor loss in accuracy usually results. A useful recommendation is to set Reltol to 0.01 for initial simulations, and then reset it to its default value of .001 when you have the simulation running the way you like it and a more accurate answer is required. Setting Reltol to a value less than .001 is generally not required.

2. Set ITL4=500 in the .OPTIONS statement.

Example: .OPTIONS ITL4=500

This increases the number of transient iterations that SPICE will attempt at each time point before it gives up. Values which are greater than 500 or 1000 won't usually bring convergence.

3. Reduce the accuracy of ABSTOL/VNTOL if current/voltage levels allow it.

Example: . OPTION ABSTOL=1N VNTOL=1M

Abstol and Vntol should be set to about 8 orders of magnitude below the level of the maximum voltage and current. The default values are Abstol=1p and Vntol=1u. These values are generally associated with IC designs.

4. Realistically Model Your Circuit; add parasitics, especially stray/junction capacitance.

The idea here is to smooth any strong nonlinearities or discontinuities. This may be accomplished via the addition of capacitance to various nodes and verifying that all semiconductor junctions have capacitance. Other tips include:

- Use RC snubbers around diodes.
- Add capacitance for all semiconductor junctions (3pF for diodes, 5pF for BJTs if no specific value is known).
- Add realistic circuit and element parasitics.
- Watch the real-time waveform display and look for waveforms that transition vertically (up or down) at the point during which the analysis halts. These are the key nodes which you should examine for problems.
- If the .Model definition for the part doesn't reflect the behavior of the device, use a subcircuit representation. This is especially important for RF and power devices such as RF BJTs and power MOSFETs. Many model vendors cheat and try to "force fit" the SPICE .MODEL statement in order to represent a device's behavior. This is a sure sign that the vendor has skimped on quality in favor of quantity. Primitive level 1 or 3 .MODEL statements CAN NOT be used to model most devices above 200MEGHz because of the effect of package parasitics. And .MODEL statements CAN NOT be used to model most power devices because of their extreme nonlinear behavior. In particular, if your vendor uses a .MODEL statement to model a power MOSFET, throw away the model. It's almost certainly useless for transient analysis.

5. Reduce the rise/fall times of the PULSE sources.

Example: VCC 1 0 PULSE 0 1 0 0 0
becomes VCC 1 0 PULSE 0 1 0 1U 1U

Again, we are trying to smooth strong nonlinearities. The pulse times should be realistic, not ideal. If no rise or fall time values are given, or if 0 is specified, the rise and fall times will be set to the TSTEP value in the .TRAN statement.

6. Add UIC (Use Initial Conditions) to the .TRAN line.

Example: .TRAN .1N 100N UIC

If you are having trouble getting the transient analysis to start because the DC operating point can't be calculated, insert the UIC keyword in the .TRAN statement (skip initial transient solution). UIC will cause PSpice to completely bypass the DC analysis. You should add any applicable .IC and IC= initial conditions statements to assist in the initial stages of the transient analysis. Be careful when you set initial conditions, for a poor setting

may cause convergence difficulties.

Modeling Tips

Device modeling is one of the hardest steps encountered in the circuit simulation process. It requires not only an understanding of the device's physical and electrical properties, but also a detailed knowledge of the particular circuit application. Nevertheless, the problems of device modeling are not insurmountable. A good first-cut model can be obtained from data sheet information and quick calculations, so the designer can have an accurate device model for a wide range of applications.

Data sheet information is generally very conservative, yet it provides a good first-cut of a device model. In order to obtain the best results for circuit modeling, follow the rule: "Use the simplest model possible." In general, the SPICE component models have default values that produce reasonable first order results. Here are some helpful tips:

- Do not make your models any more complicated than they need to be. Overcomplicating a model will only cause it to run more slowly and will increase the likelihood of an error.
- Remember: modeling is a compromise.
- Don't be afraid to pull apart your circuit and test individual sections or even models, especially the ones you did not create.

- Create subcircuits which can be run and debugged independently. Simulation is just like being at the bench. If the simulation of the entire circuit fails, you should break it apart and use simple test circuits to verify the operation of each component or section.
- Document the models as you create them. If you do not use a model often, you might forget how to use it.
- Be careful when using models which have been produced by hardware vendors. Many have limitations on the operating point bounds for which they can be used.
- Semiconductor models should always include junction capacitance and the transit time (AC charge storage) parameters.
- If the .Model definition for a large geometry device doesn't reflect the behavior of the device, use a subcircuit representation.
- Be careful when using behavioral models for power devices. Many models are not thoroughly tested and work at one operating point but are highly inaccurate at other operating points.

- And lastly, there is no substitute for knowing what you're doing!!

Chapter 4 - Library Listings

Please see the file Power_Library_List_4.5.pdf and XLS files for an electronic version of these listings.

An asterisk (*) or red entry in the left column indicates that the model has been recently added.

You can sort by Library Version in order to see what models have recently been added.

Chapter 5 - References

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