NCS2006 SPICE Model Report

1.0 Scope

This report compares the simulated performance of the NCS2006 Rail-to-Rail Input and Output, 3MHz opamp to the specifications and data provided by ON Semiconductor.

2.0 Op-amp Performance Features Included in this SPICE Model

Effects we are going to be modeling (All tests are at specific supply voltage, temperature and load current, unless otherwise noted)

- AC Gain/Phase vs. Frequency
- Input Common Mode Impedance vs. Frequency
- Input Differential Mode Impedance vs. Frequency
- Input Bias / Input Offset Bias Currents vs. Temperature
- AC Common Mode Rejection Ratio (CMRR) vs. Frequency
- DC Common Mode Input Range
- AC Power Supply Rejection Ratio Plus (PSRR) vs. Frequency
- AC Power Supply Rejection Ratio Minus (PSRR) vs. Frequency
- Closed Loop Output Impedance vs. Frequency
- Output Short Circuit (Sinking) Current vs. Power Supply Voltage
- Output Short Circuit (Sourcing) Current vs. Power Supply Voltage
- Output Voltage Saturation Plus (VDD - VOH)) vs. Output Current
- Output Voltage Saturation Minus (VOL - VSS)) vs. Output Current
- DC Saturation
- Slew Rate vs. Temperature at VDD Max (Configured as a Comparator)
- Slew Rate vs. Temperature at VDD Min (Configured as a Comparator)
- Small Signal Pulse Response (Inverting)
- Small Signal Pulse Response (Non-Inverting)
- Large Signal Pulse Response (Non-Inverting)
- Large Signal Pulse Response (Inverting)
- Quiescent Current vs. Power Supply Voltage
- Input Noise Voltage Density vs. Frequency
- Offset Voltage Drift with temperature at 25C, offset voltage set to 0 volts
- Single Ended Large Signal (Non-Inverting)

Effects we are NOT going to be modeling

- Input Bias Current vs. Common Mode Input Voltage
- Input Noise Voltage Density vs. Common Mode Input Voltage
- CMRR vs. Temperature
- PSRR vs. Temperature
- Input Offset Voltage vs. Common Mode Input Voltage
- Input Offset Voltage vs. Output Voltage
- Input Offset Voltage vs. Power Supply Voltage
- Quiescent Current vs. Common Mode Input Voltage
- DC Open Loop Gain vs. Temperature
- GBWP, Phase Margin vs. Temperature
- Output Voltage Swing vs. Frequency
- Output Voltage Headroom vs. Temperature
- Measured Input Current vs. Input Voltage

3.0 Functional Description

The NCS2006 series operational amplifiers provide rail−to−rail input and output operation, 3 MHz bandwidth, and are available in single, dual, and quad configurations. Rail−to−rail operation gives designers use of the entire supply voltage range while taking advantage of the 3 MHz bandwidth. The NCS2006 can operate on supply voltages from 1.8 to 5.5 V over a temperature range from −40 to 125°C. At a 1.8 V supply, this device has a slew rate of 1.2 V/us while consuming only 125uA of quiescent current per channel. Since this is a CMOS device, high input impedance and low bias currents make it ideal for interfacing to a wide variety of signal sensors. The NCS2006 devices are available in a variety of compact packages.

Features

- Rail−to−rail Input and Output
- Wide Supply Range: 1.8V to 5.5V
- Wide Bandwidth: 3MHz
- High Slew Rate: 1.2 V/μs at Vs=1.8V
- Low Quiescent Current: 125uA per Channel at Vs = 1.8V
- Low Input Bias Current: 1pA Typical
- Wide Temperature Range: −40 to 125°C
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Unity Gain Buffer
- Battery Powered / Low Quiescent Current Applications
- Low Cost Current Sensing
- Automotive

4.0 Model Packaging Pin Connections

```
.SUBCKT NCS2006 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*               Non-inverting Input
```

5.0 Model Verification Testing

5.1.1 AC Gain/ Phase

1_AC_G2_MARGIN-ACGAIN

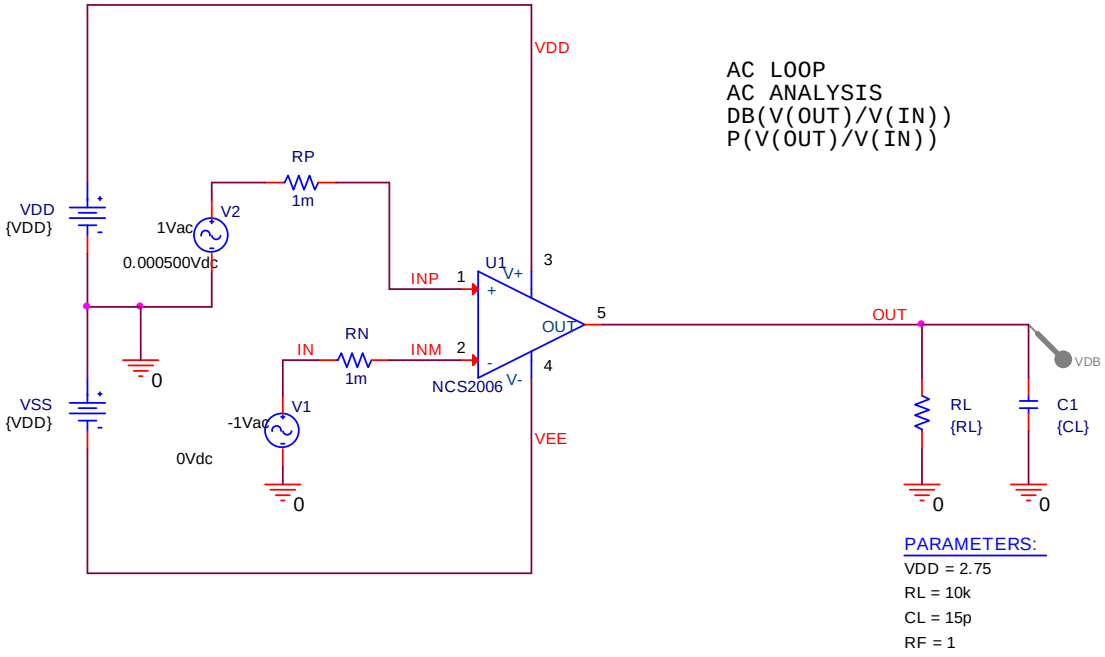

Figure 5-1 AC Gain/ Phase Test Circuit

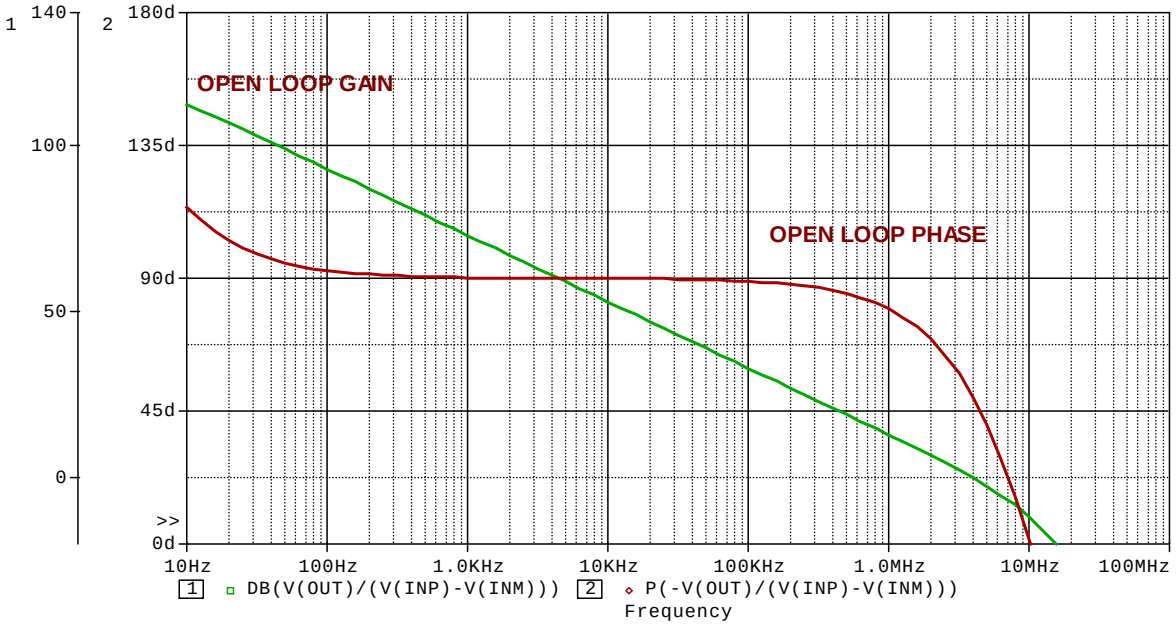

Figure 5-2 AC Gain/ Phase Test Results

5.1.2 Common Mode Impedance AC Analysis

2_COM_MODE_INPUT_Z

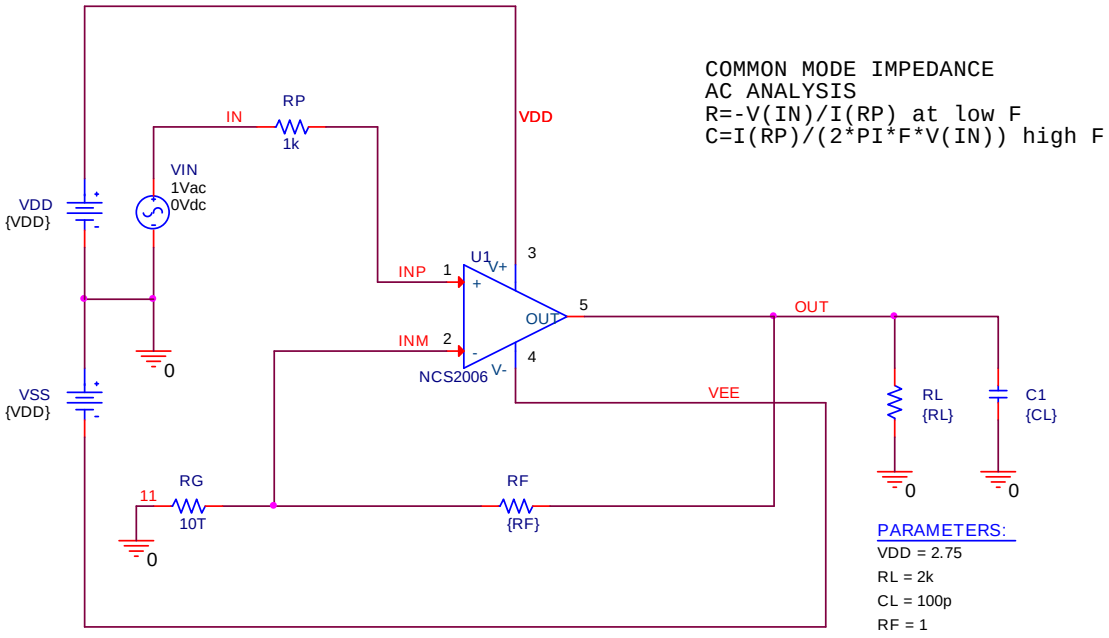

Figure 5-3 Common Mode Impedance AC Analysis Test Circuit

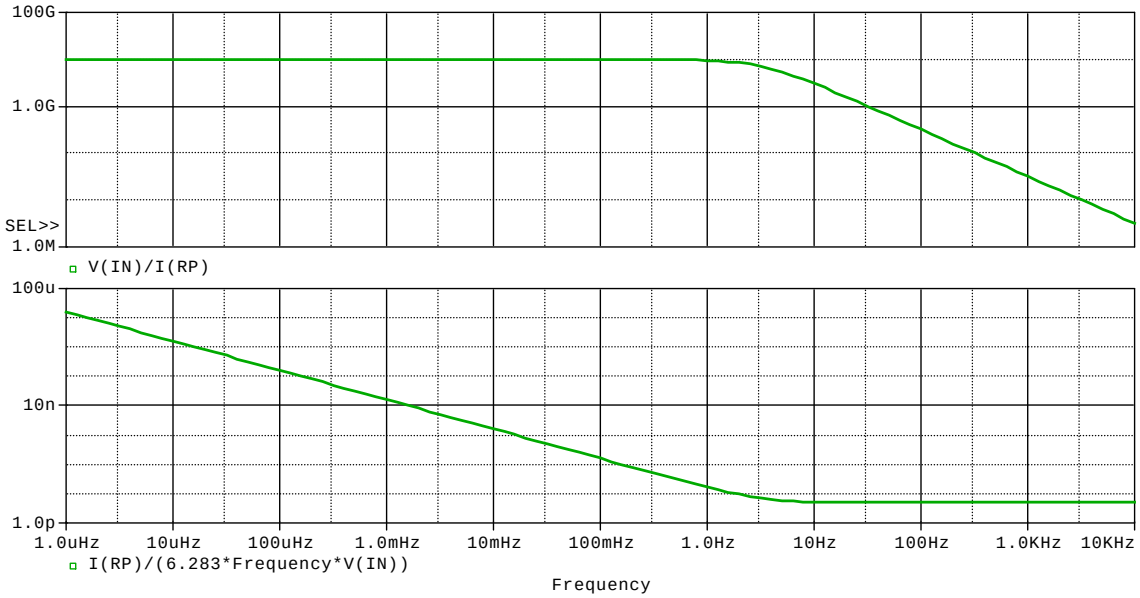

Figure 5-4 Common Mode Impedance AC Analysis Test Results

5.1.3 Differential Mode Input Impedance AC Analysis

3_DIFF_MODE_INPUTZ

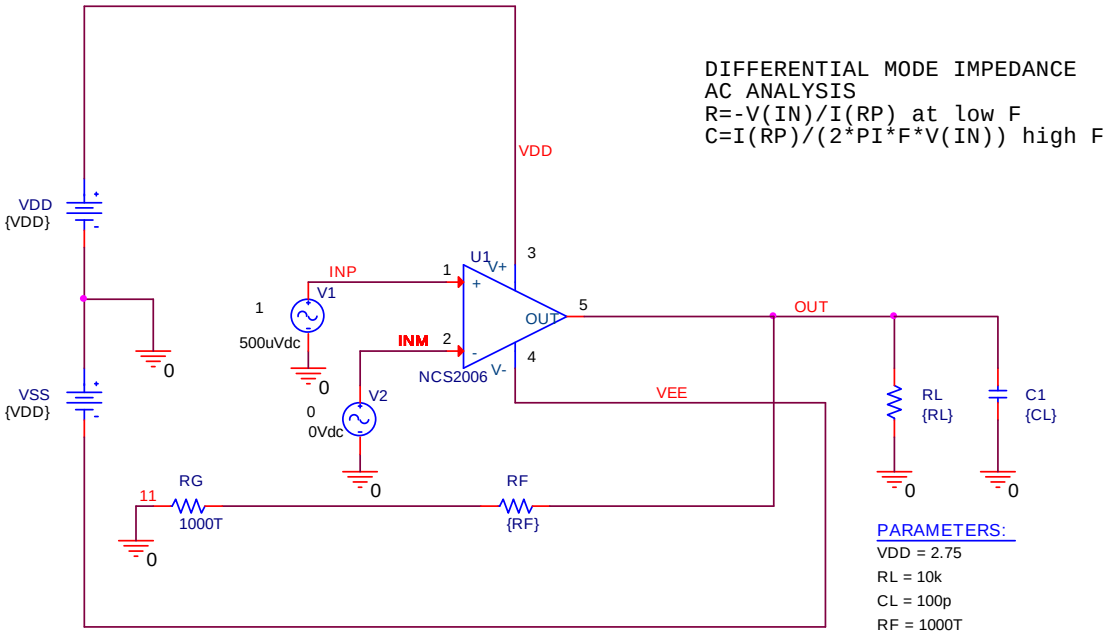

Figure 5-5 Differential Mode Impedance Test Circuit

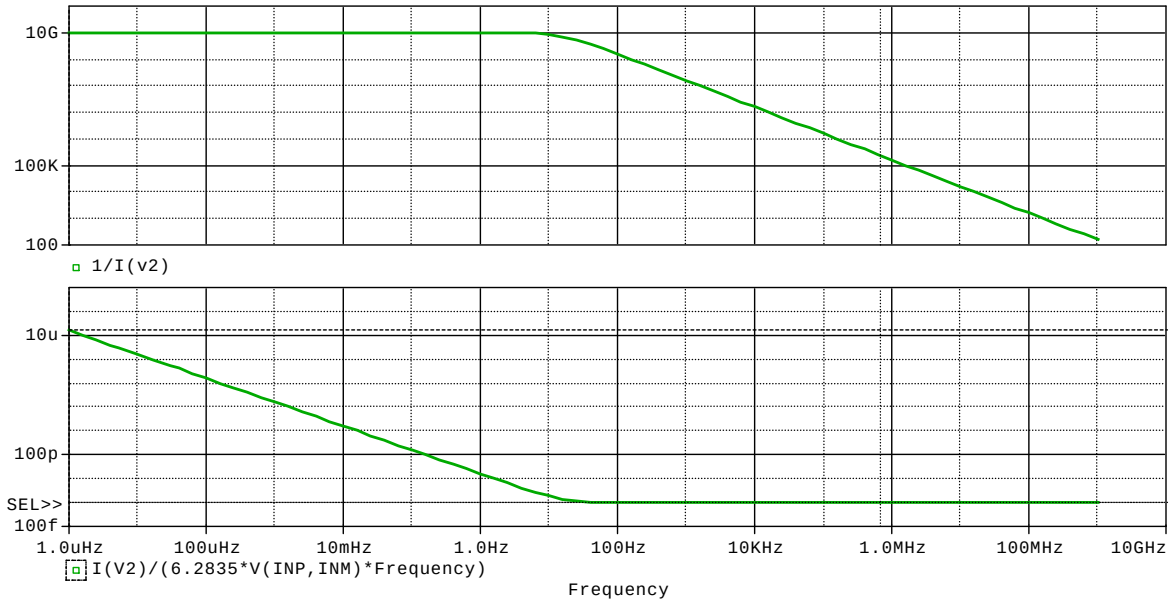

Figure 5-6 Differential Mode Impedance Test Results

5.1.4 Input Bias Current vs. Temperature

4_IB_VS_T

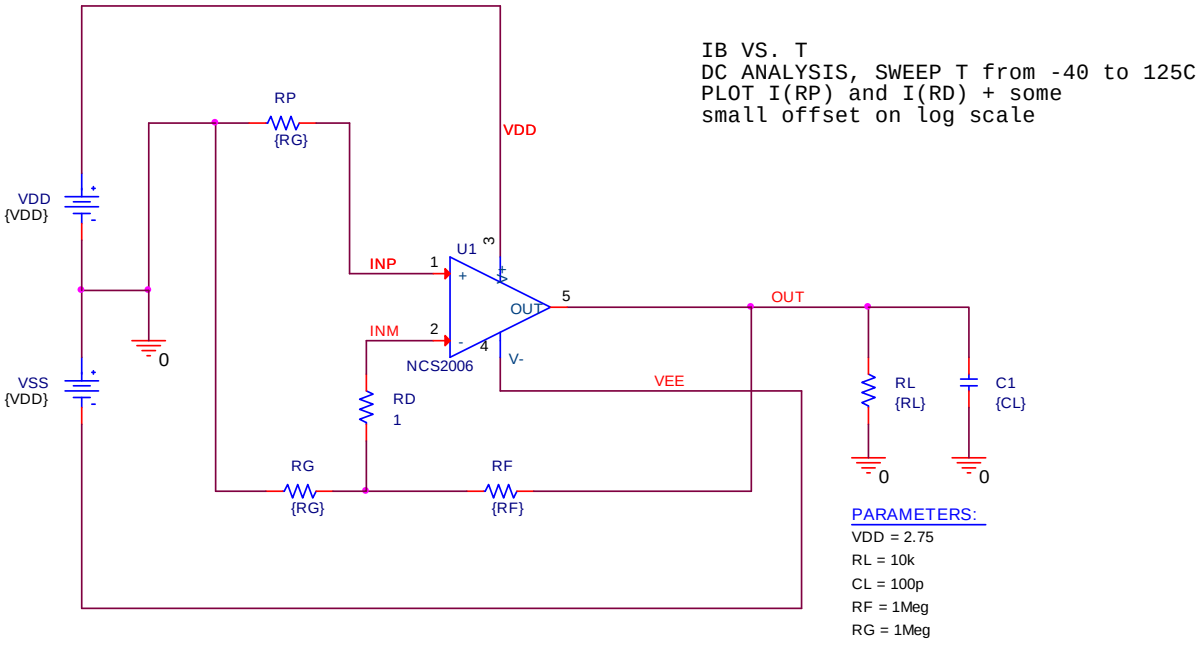

Figure 5-7 Input Bias Current vs. Temperature Test Circuit

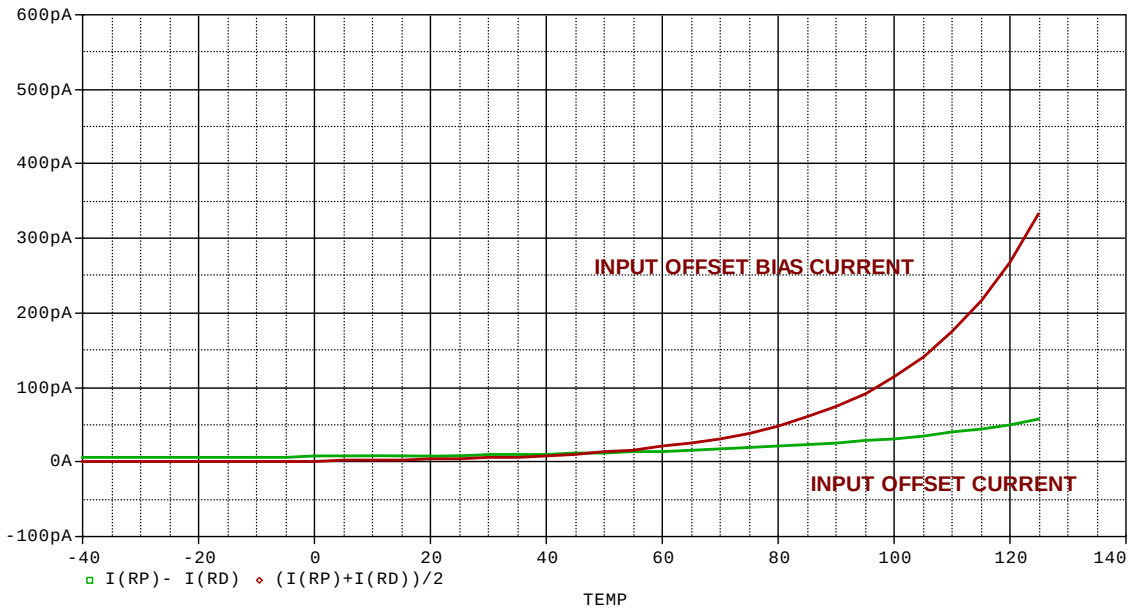

Figure 5-8 Input Bias Current vs. Temperature Test Results

5.1.5 CMRR vs. Frequency

5_AC_CMRR

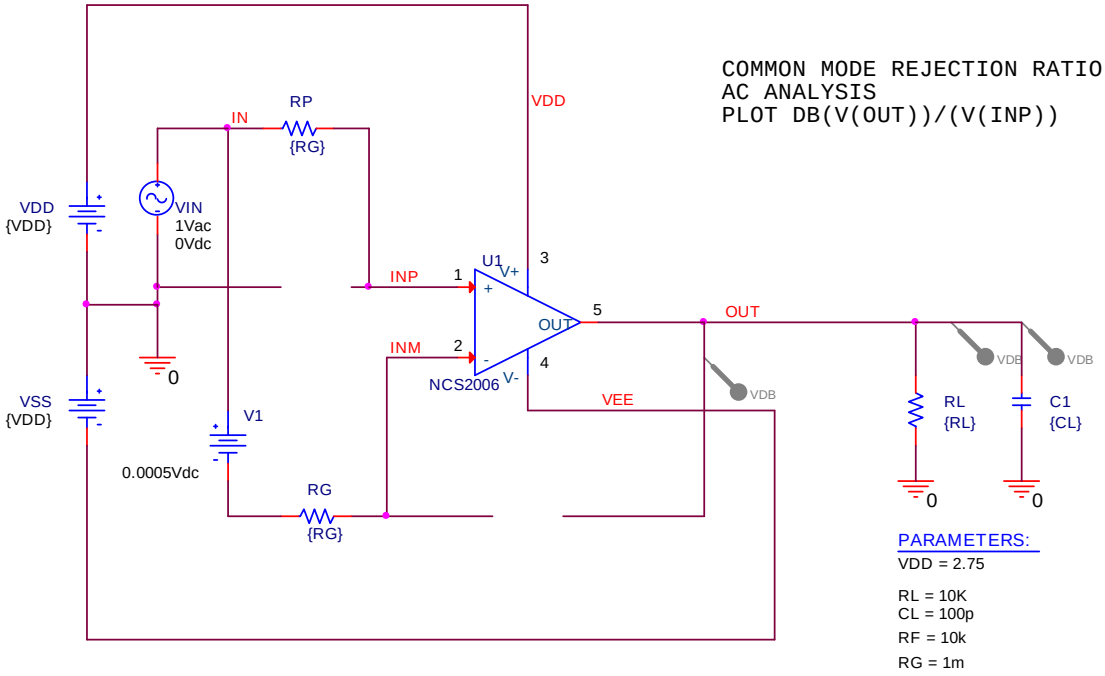

Figure 5-9 CMRR vs. Frequency Test Circuit

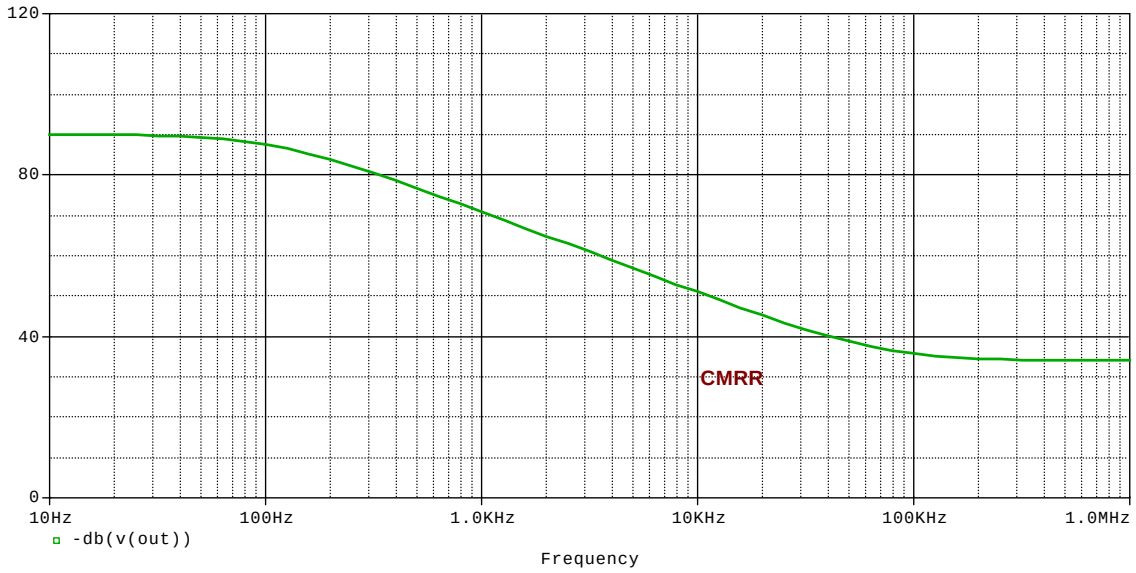

Figure 5-10 CMRR vs. Frequency Test Results

5.1.6 Common Mode Input Range DC

6_COM_MODE_INP_RANGE

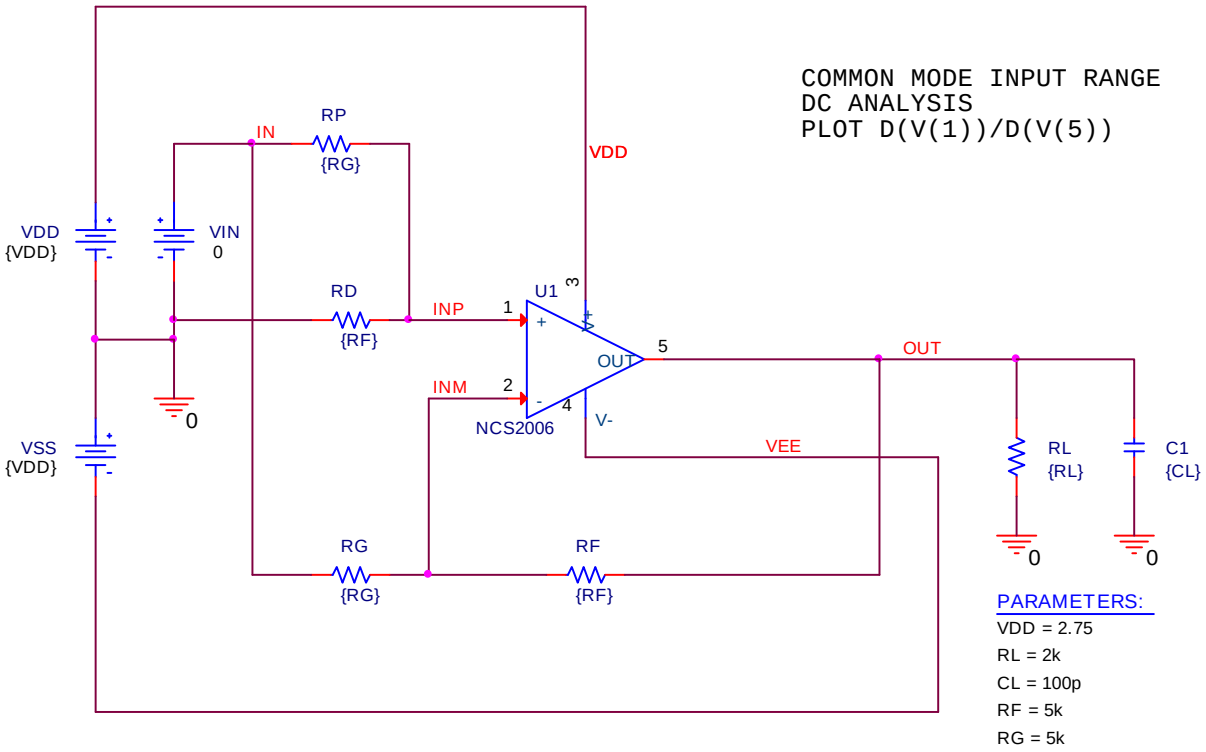

Figure 5-11 Common Mode Input Range DC Analysis Test Circuit

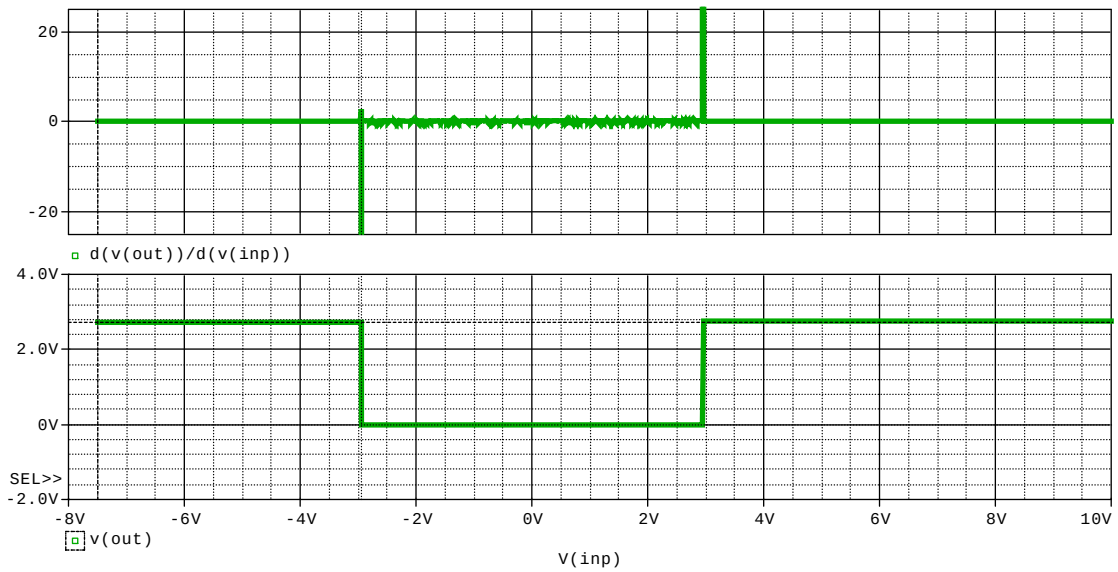

Figure 5-12 Common Mode Input Range DC Analysis Test Results

5.1.7 PSRR Plus Supply

7_AC_PSRR_PLUS-7_ PSRR_PLUS

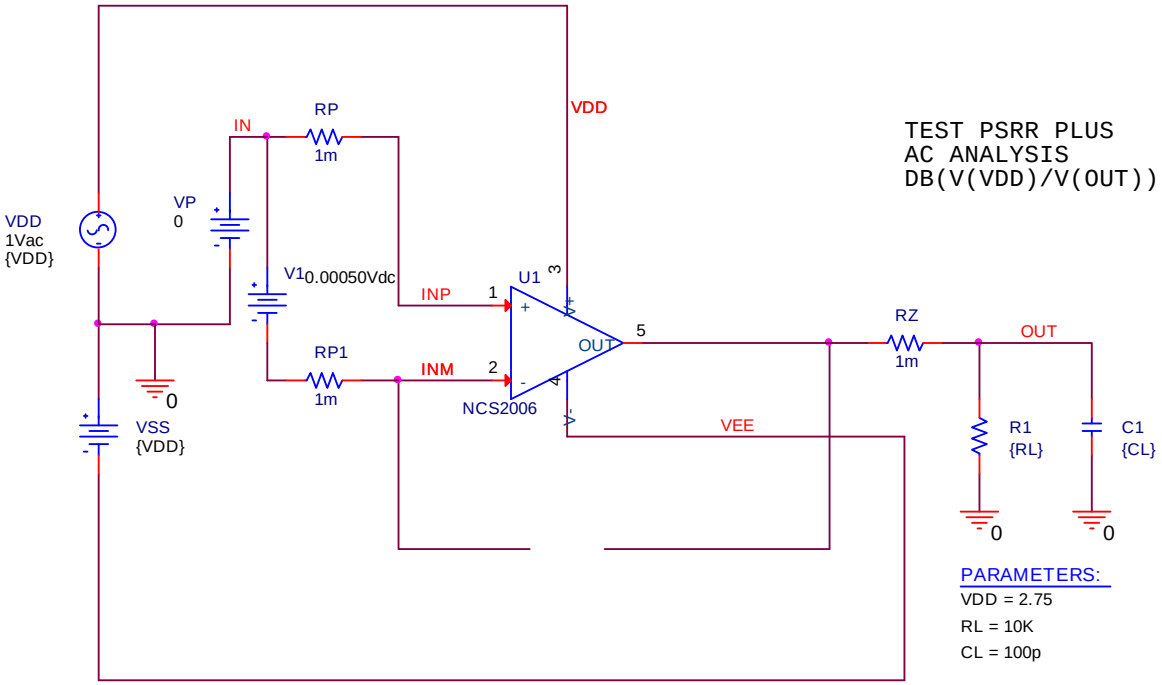

Figure 5-13 PSRR Plus Test Circuit

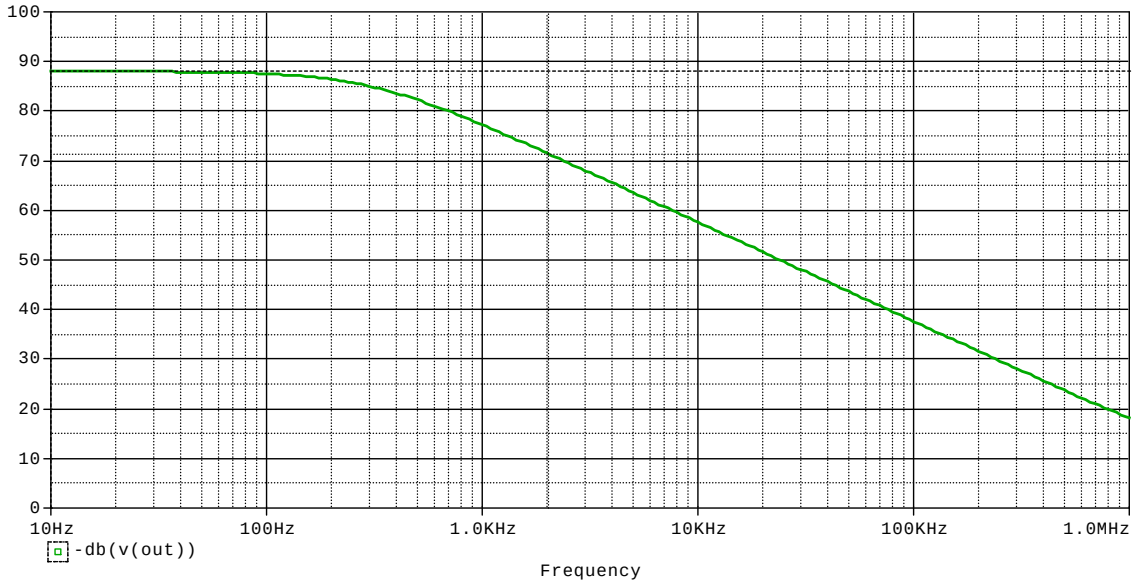

Figure 5-14 PSRR Plus Test Results

5.1.8 PSRR Minus Supply

8_AC_PSRR_MINUS

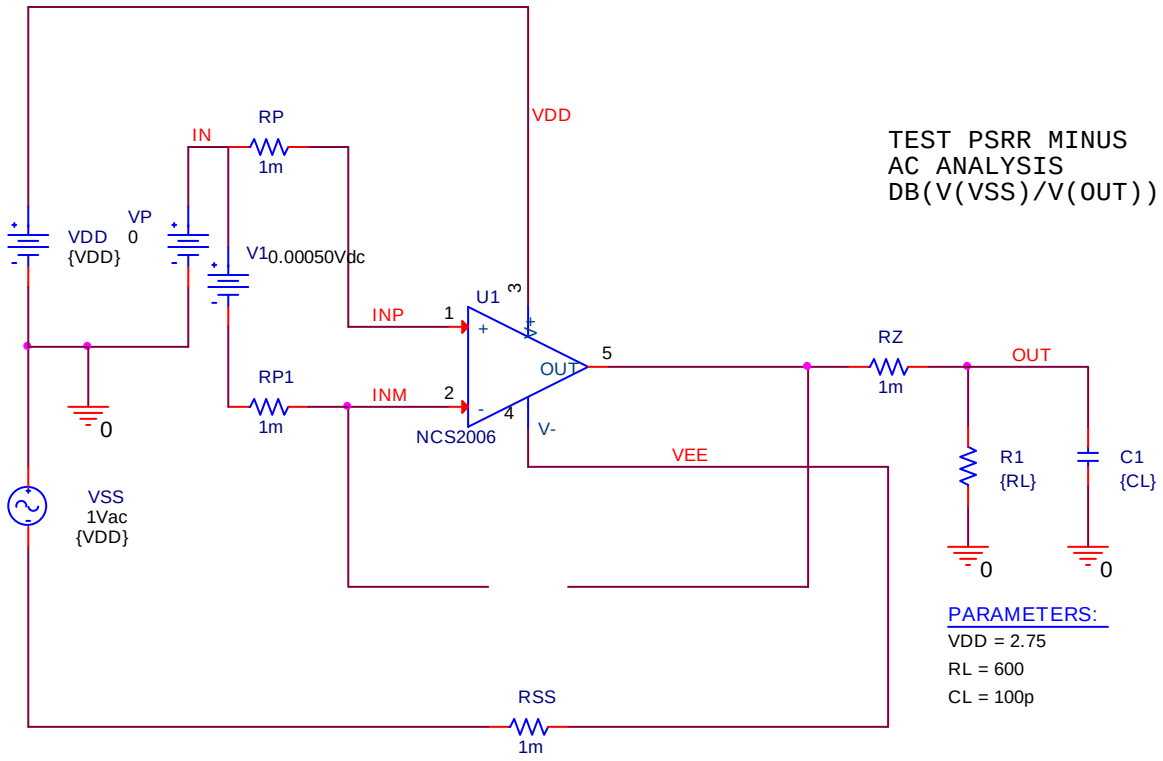

Figure 5-15 PSRR Minus Test Circuit

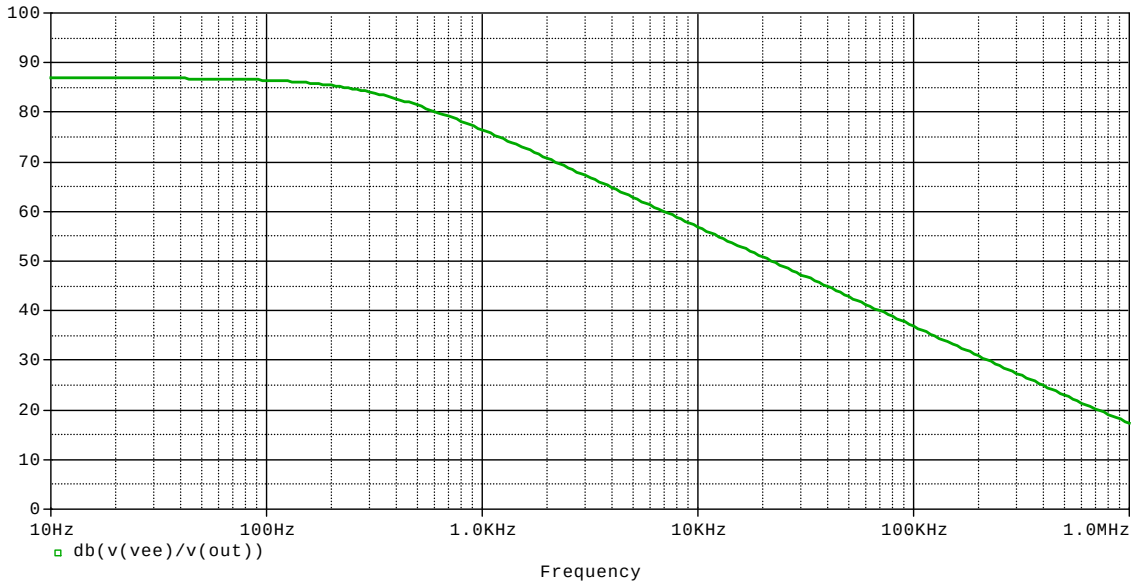

Figure 5-16 PSRR Minus Test Results

5.1.9 Output Impedance

9_ROUT

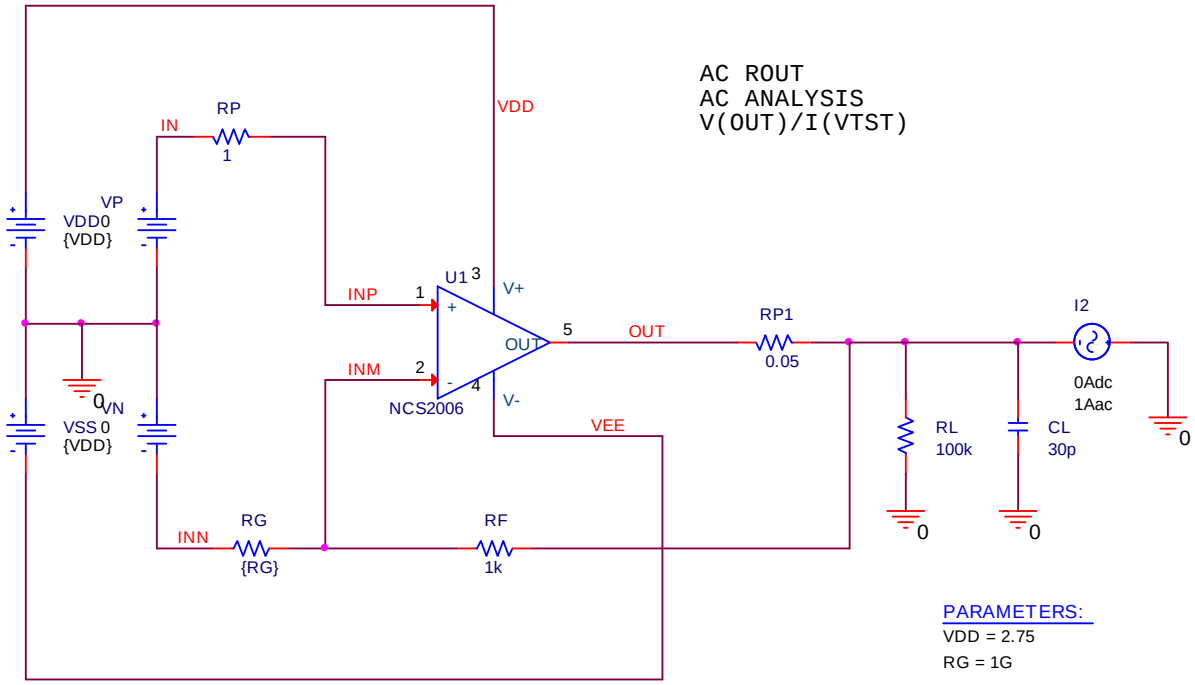

Figure 5-17 Output Impedance Test Circuit

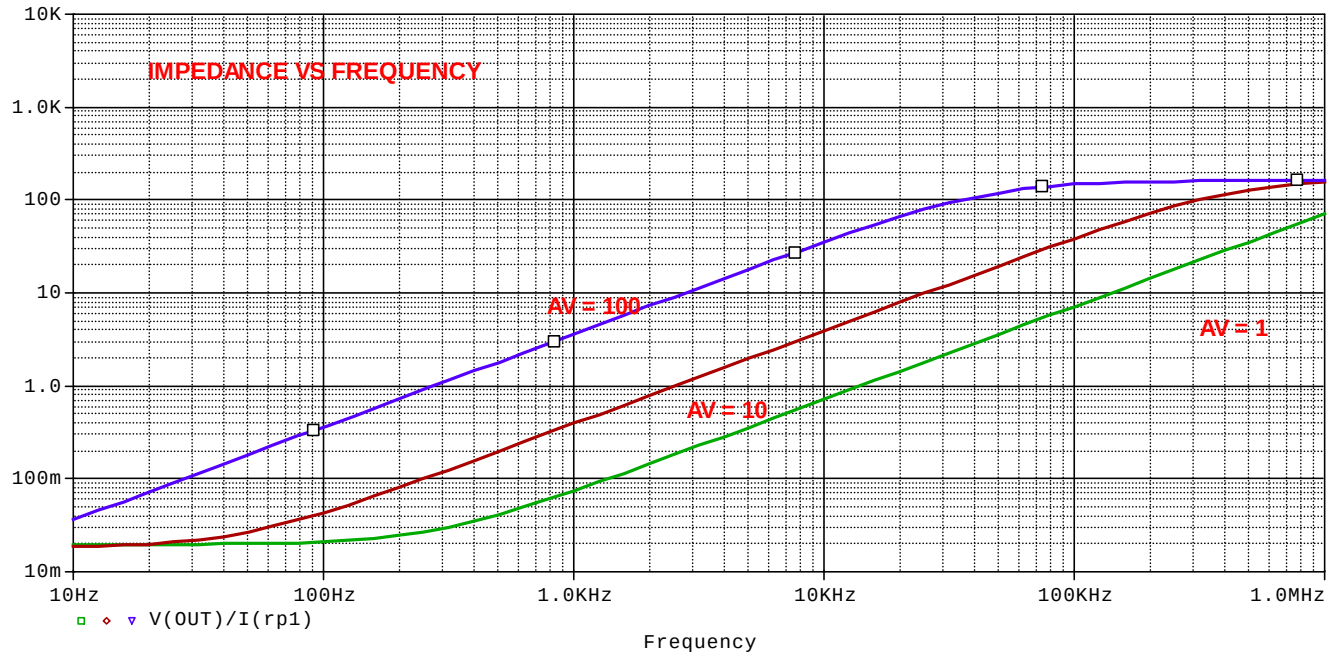

Figure 5-18 Output Impedance Test Results

5.1.10 Short Circuit Current Sinking

10A_SHORTCKT_SINKING

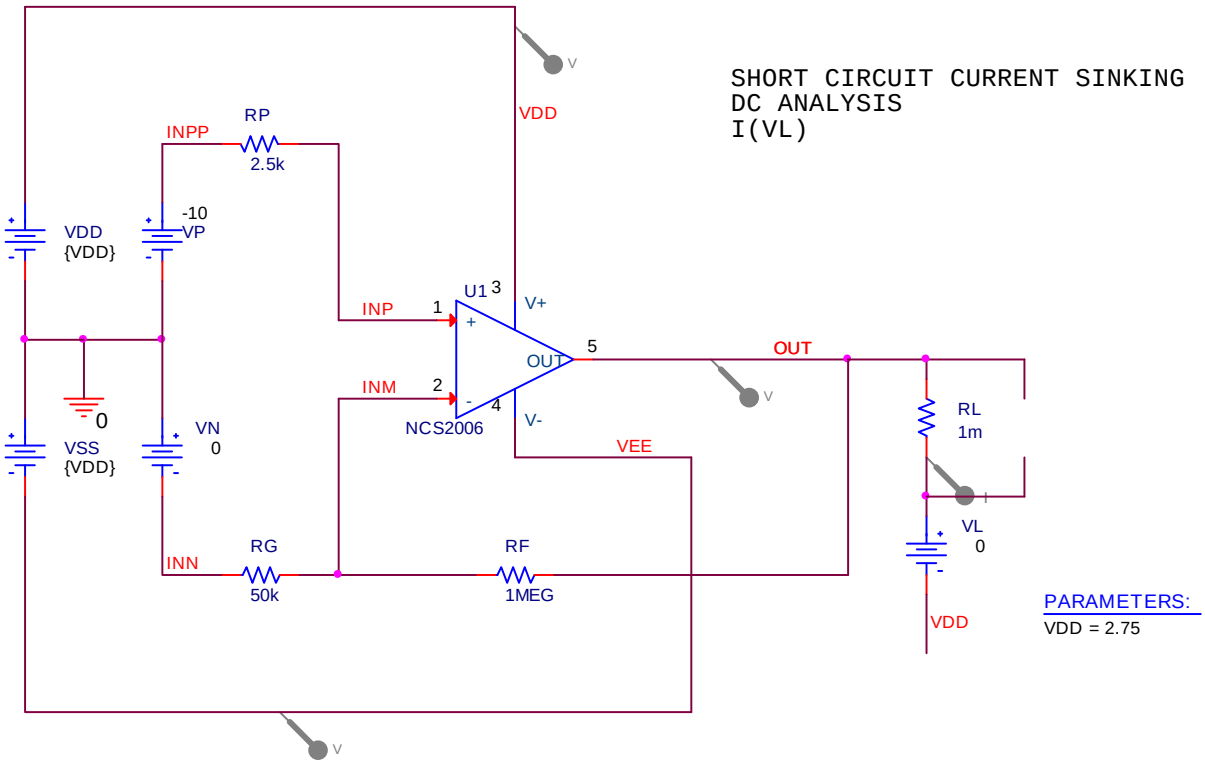

Figure 3-19 Short Circuit Current Sinking Test Circuit

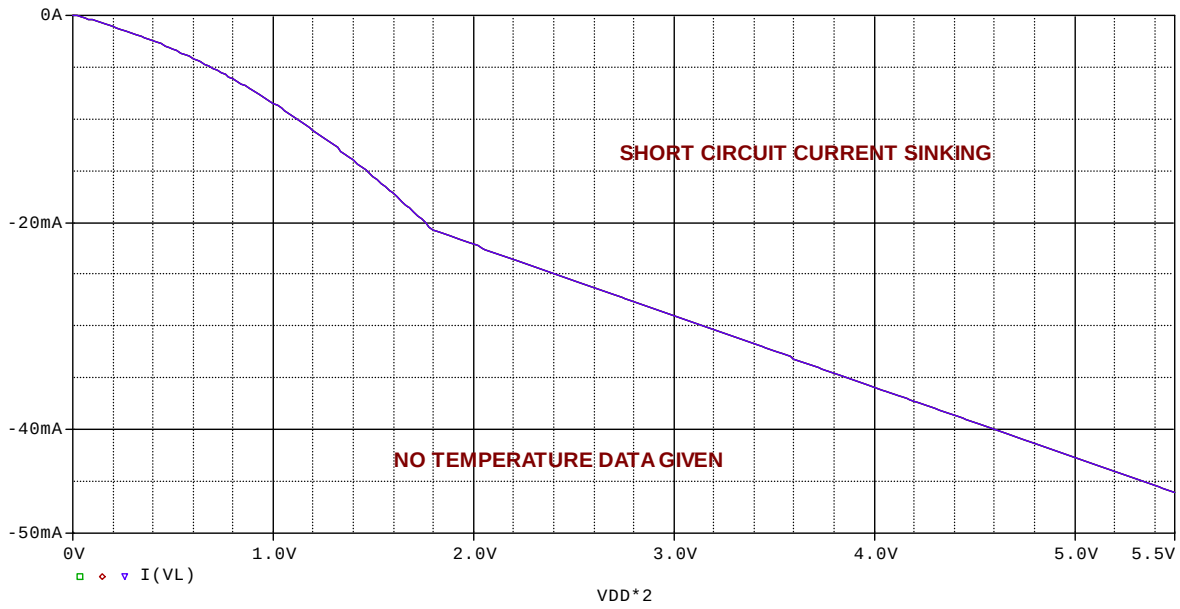

Figure 3-20 Short Circuit Current Sinking Test Results

5.1.11 Short Circuit Current Sourcing

10B_SHORTCKT_SOURCING

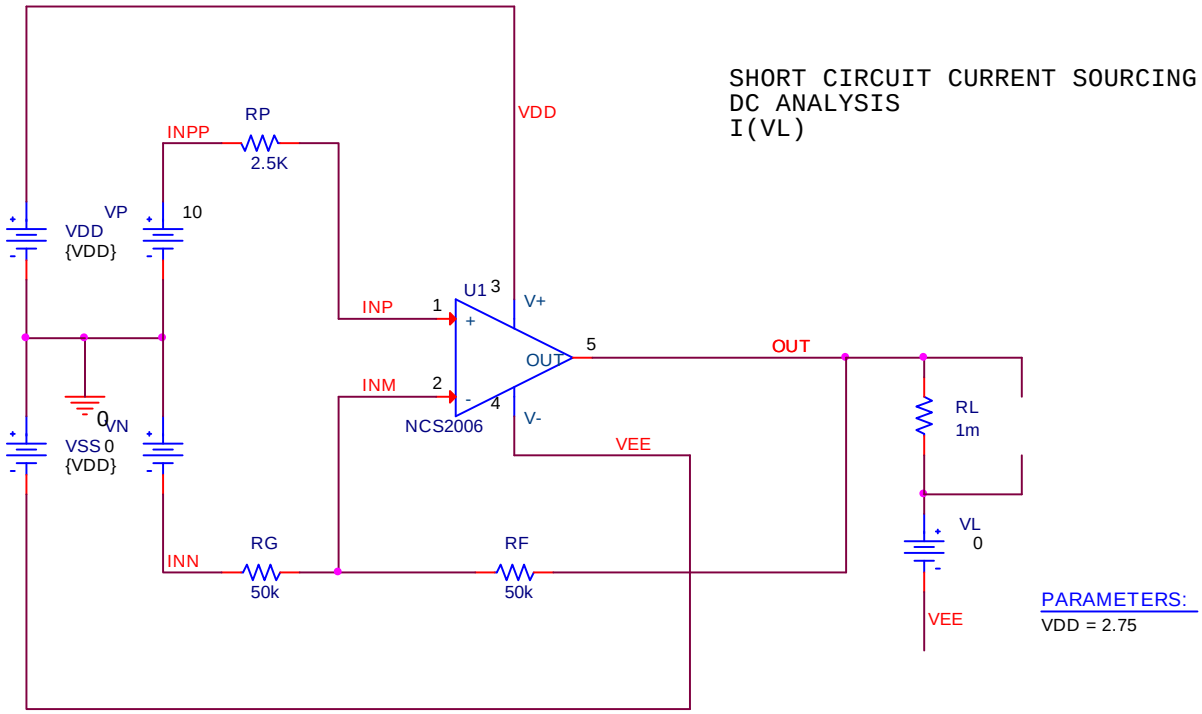

Figure 3-21 Short Circuit Current Sourcing Test Circuit

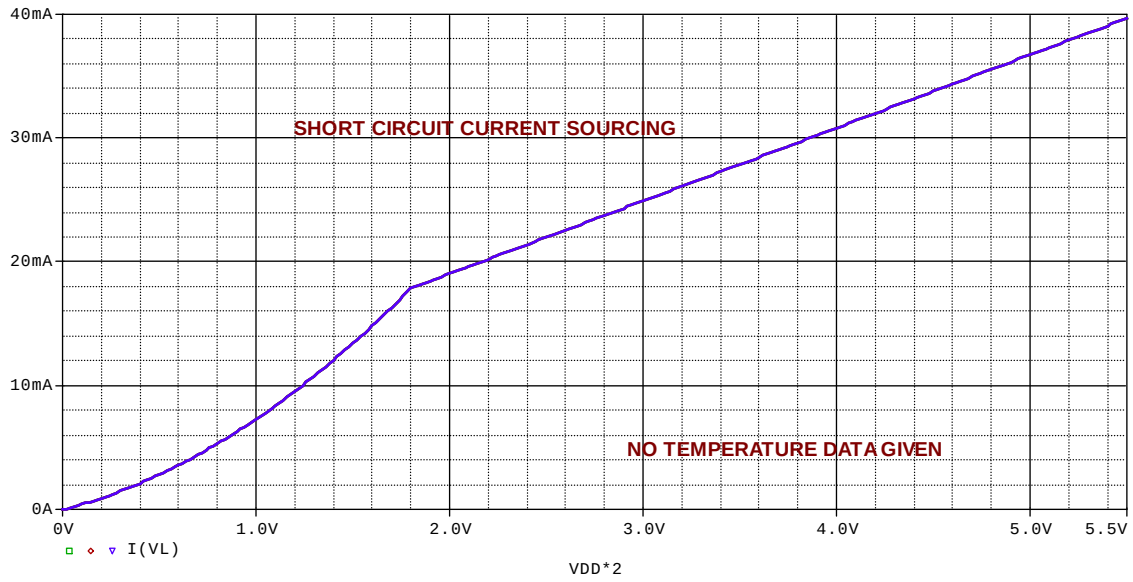

Figure 3-22 Short Circuit Current Sourcing Test Results

5.1.12 VSat Plus Supply

11_VSAT_PLUS

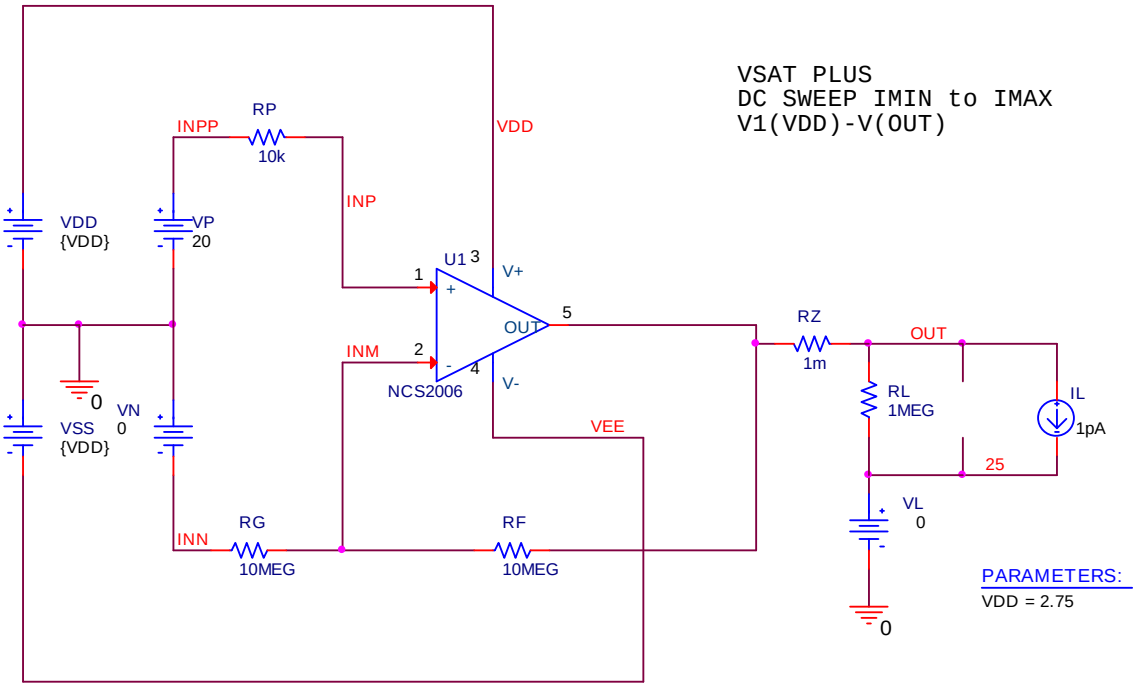

Figure 3-23 VSat Plus Test Circuit (Vs = 5.5V)

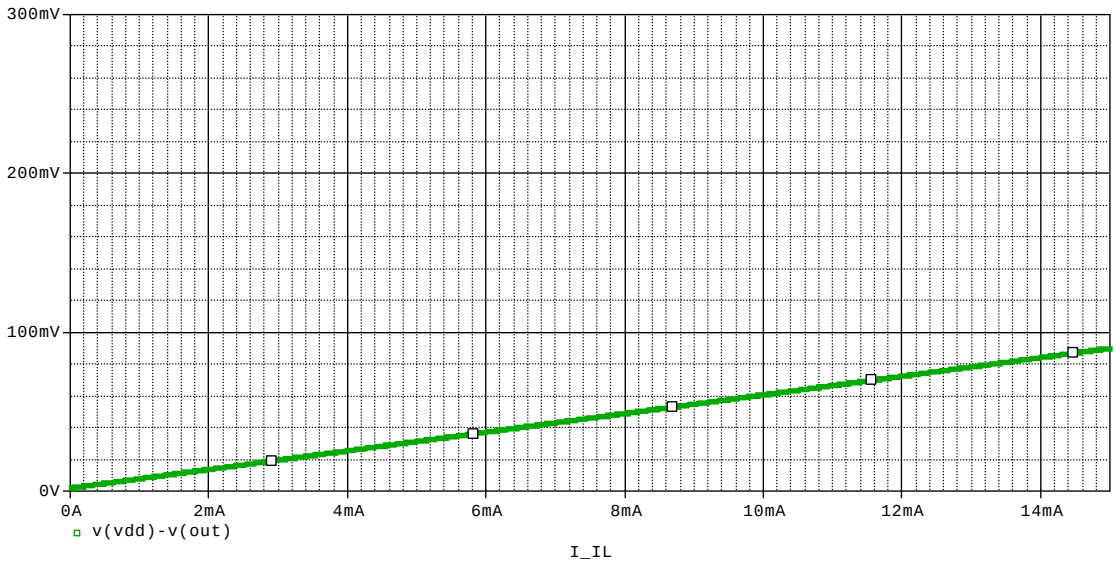

Figure 3-24 VSat Plus Test Results (Vs = 5.5V)

5.1.13 VSat Minus Supply

12_VSAT_MINUS

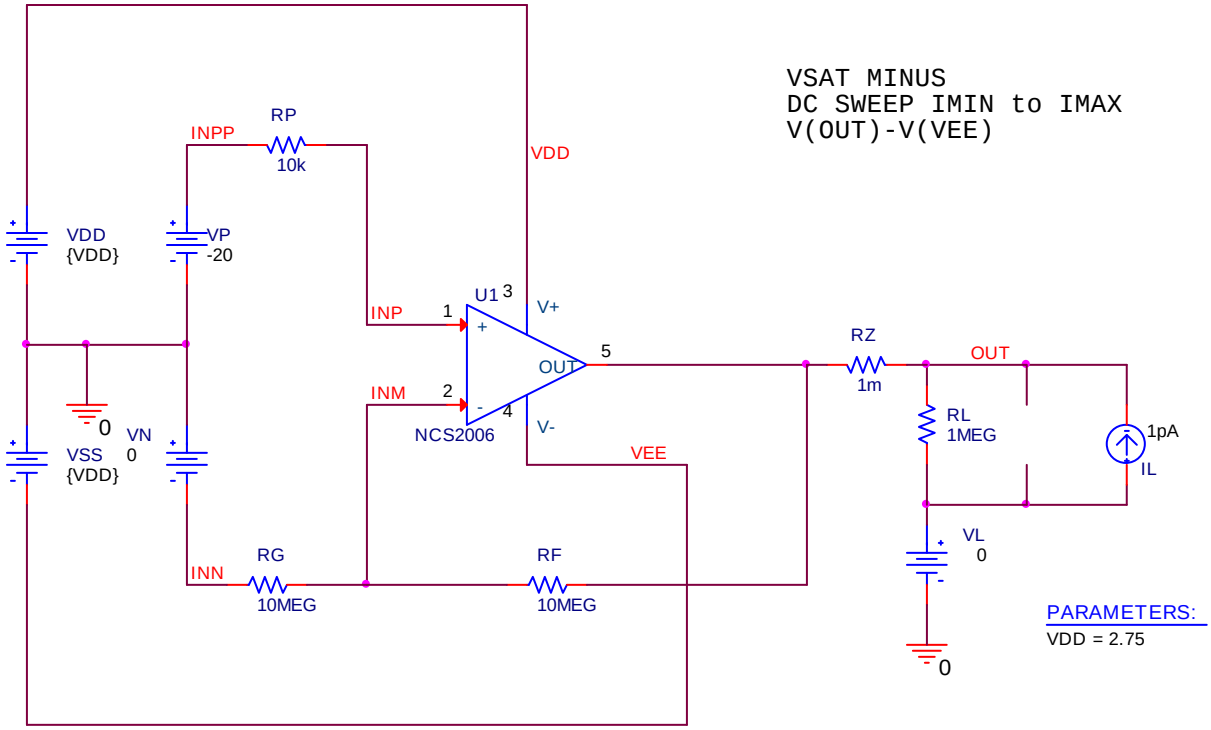

Figure 3-25 VSat Minus Test Circuit (Vs = 5.5V)

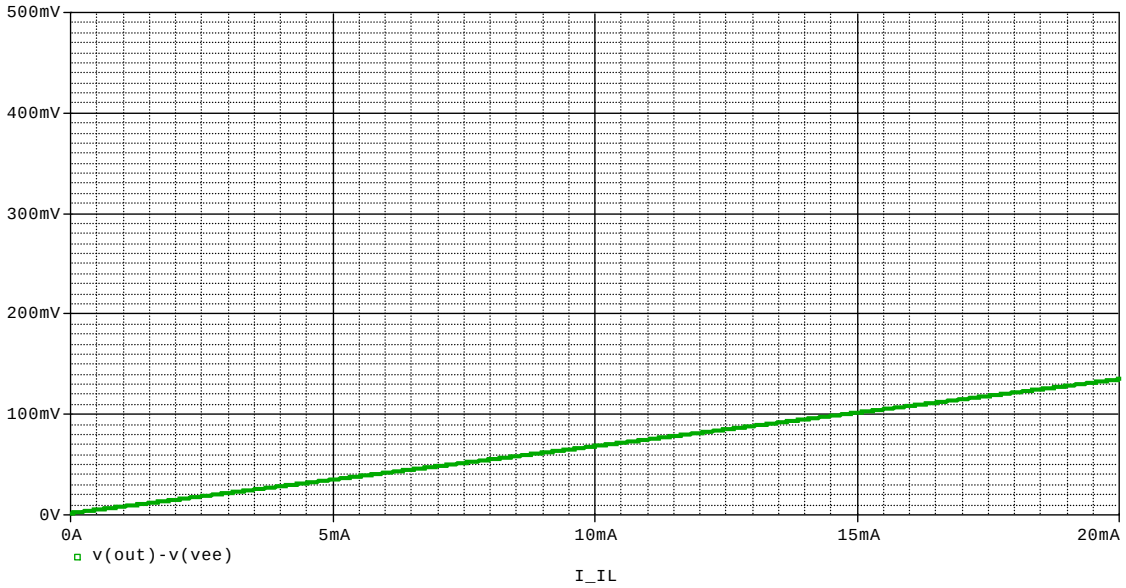

Figure 3-26 VSat Minus Test Results (Vs = 5.5V)

5.1.14 Output Voltage Swing

13_DCSAT-DCSAT

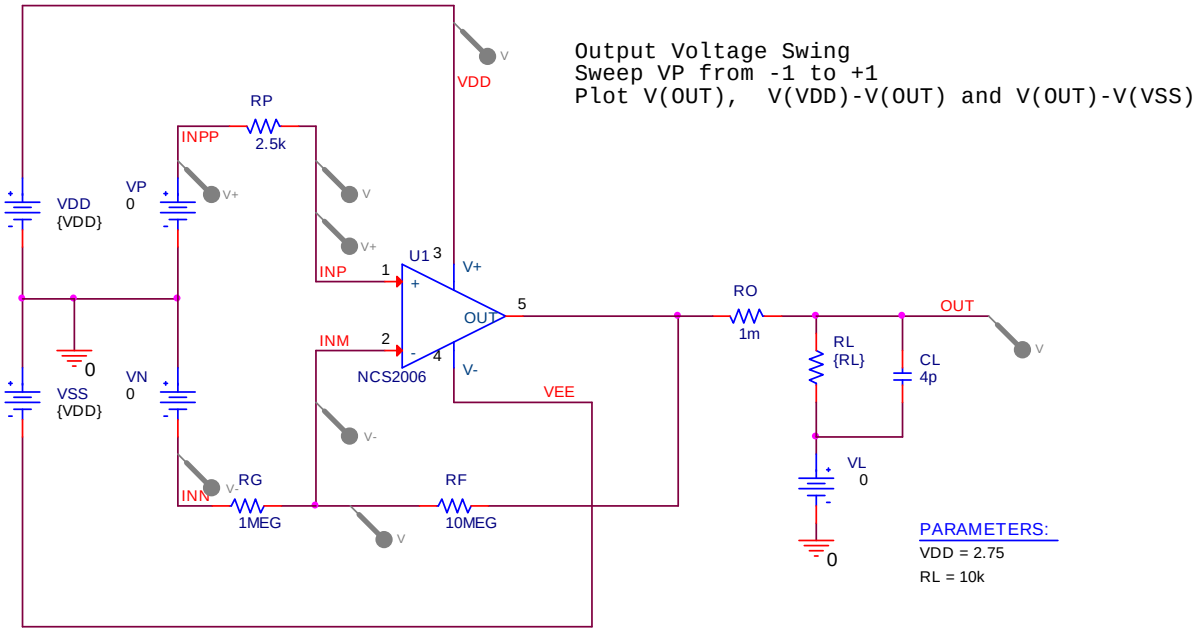

Figure 3-27 Output Voltage Swing Sweep Test Circuit

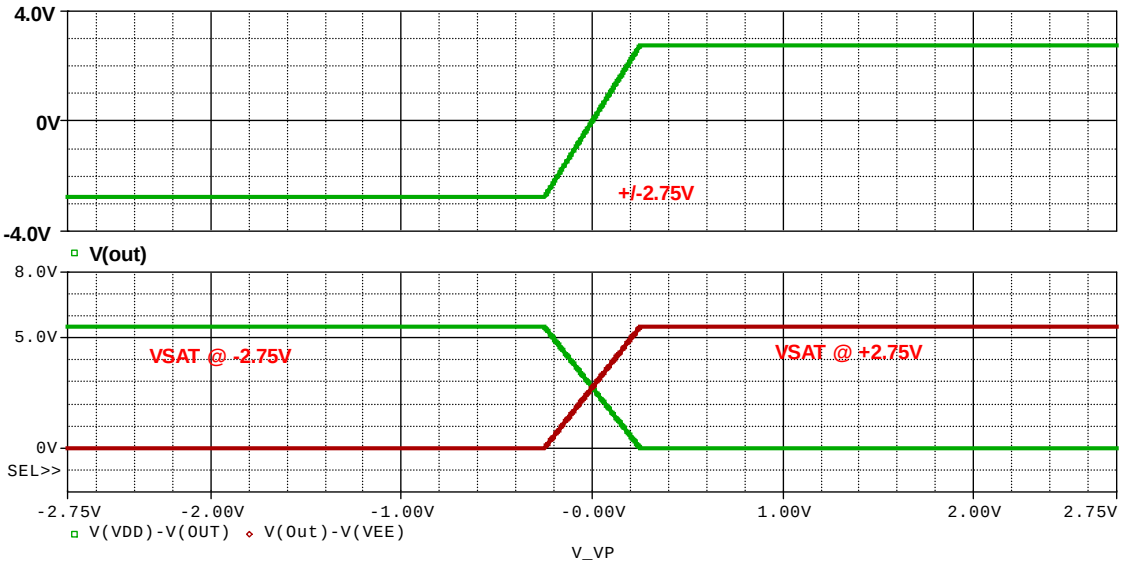

Figure 3-28 Output Voltage Swing Sweep Test Results

5.1.15 Slew Rate Vdd +/-2.75V

14_SLEW_RATE-14_SLEW_RATE

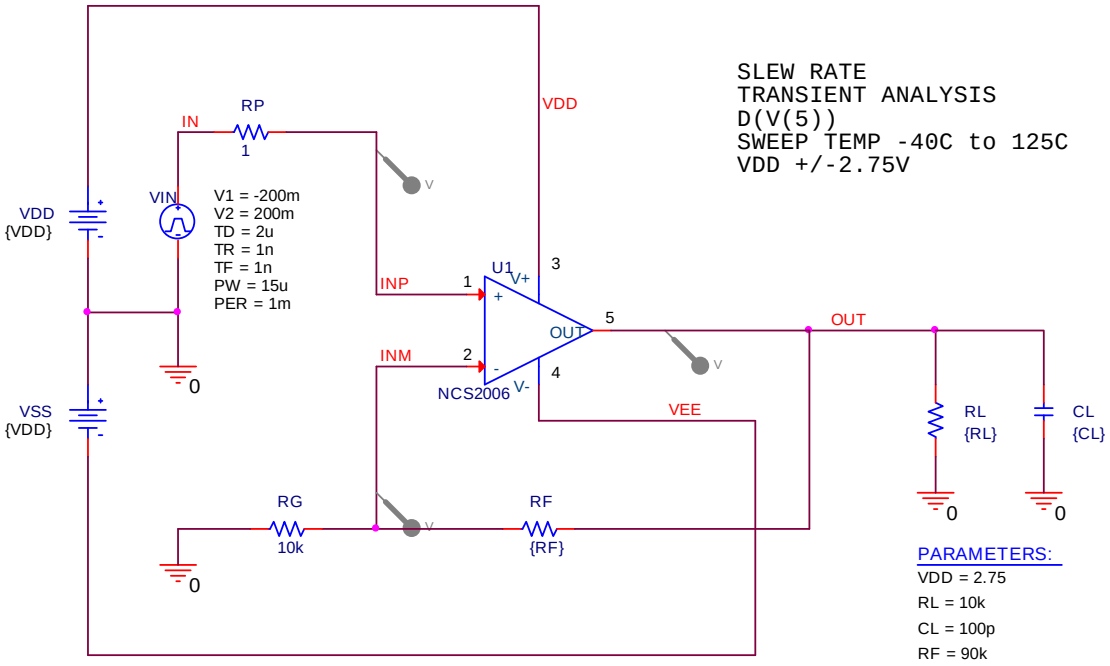

Figure 3-29 Slew Rate (Vdd=+/-2.75v) Test Circuit

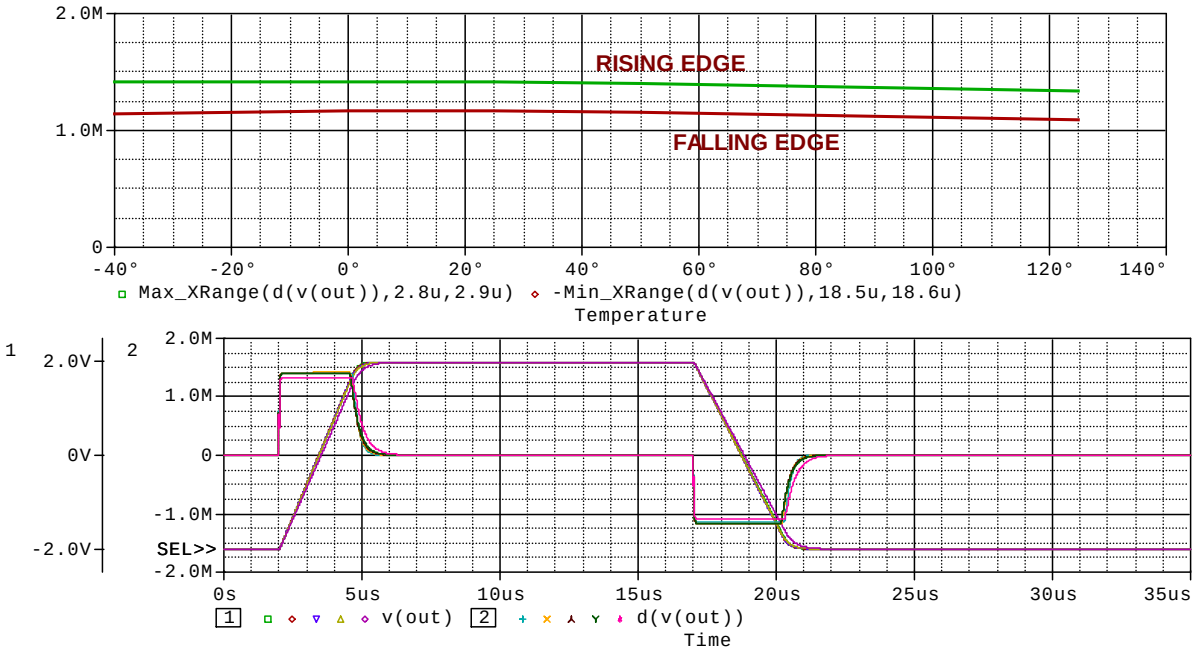

Figure 3-30 Slew Rate (Vdd=+/-2.75v) Test Results

5.1.16 Small Signal Non-Inverting Pulse Response

15_SSPULSE

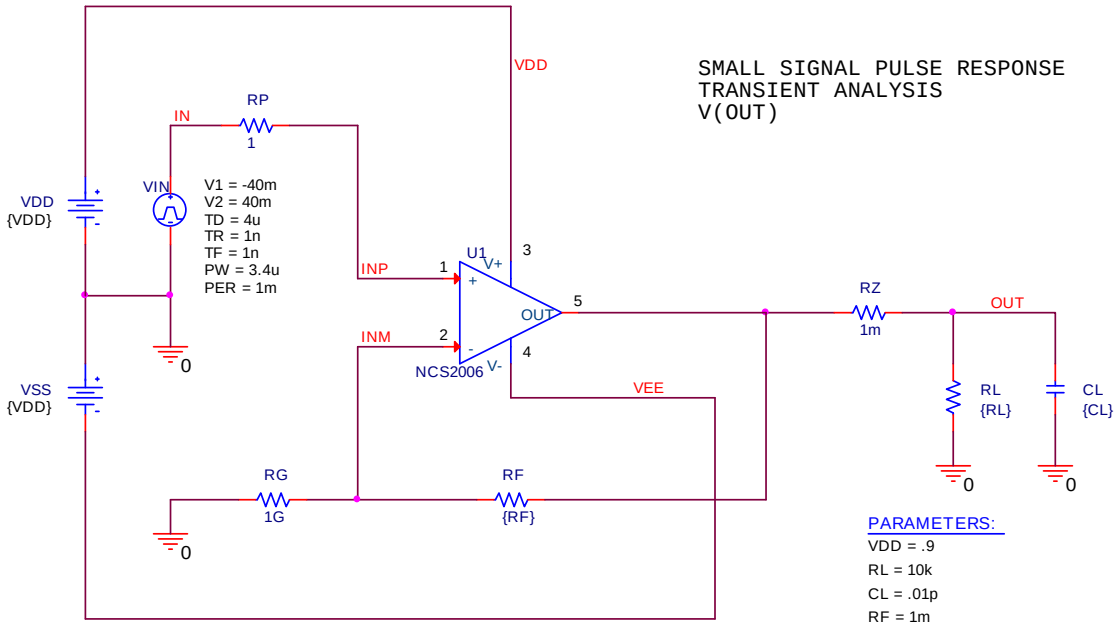

Figure 3-33 Small Signal Non-Inverting Test Circuit

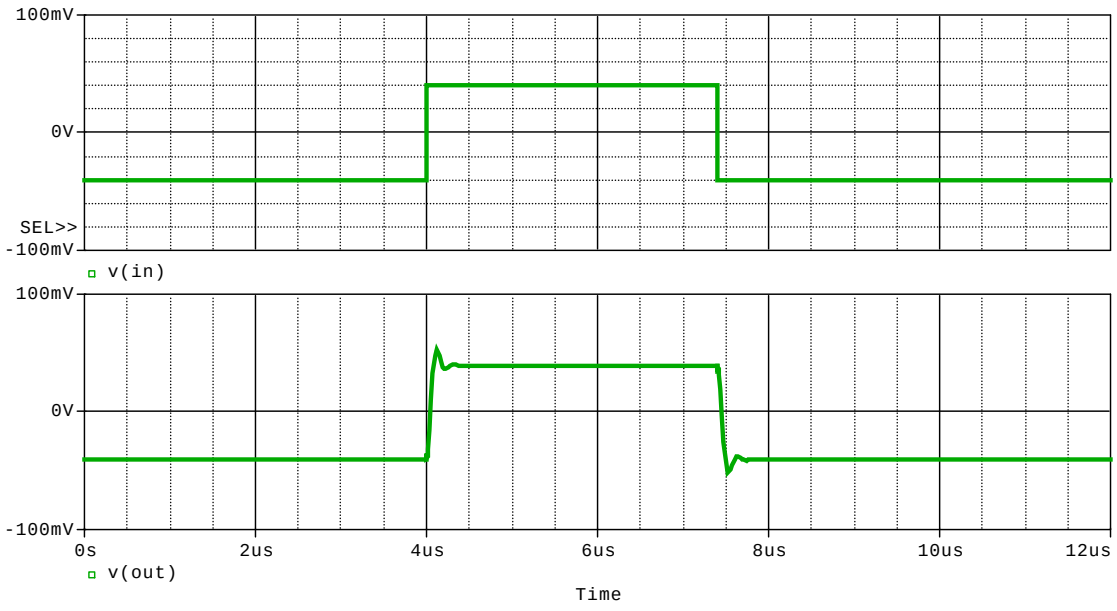

Figure 3-34 Small Signal Non-Inverting Test Results

5.1.17 Small Signal Inverting Pulse Response

15_SSPULSE_INVERTING

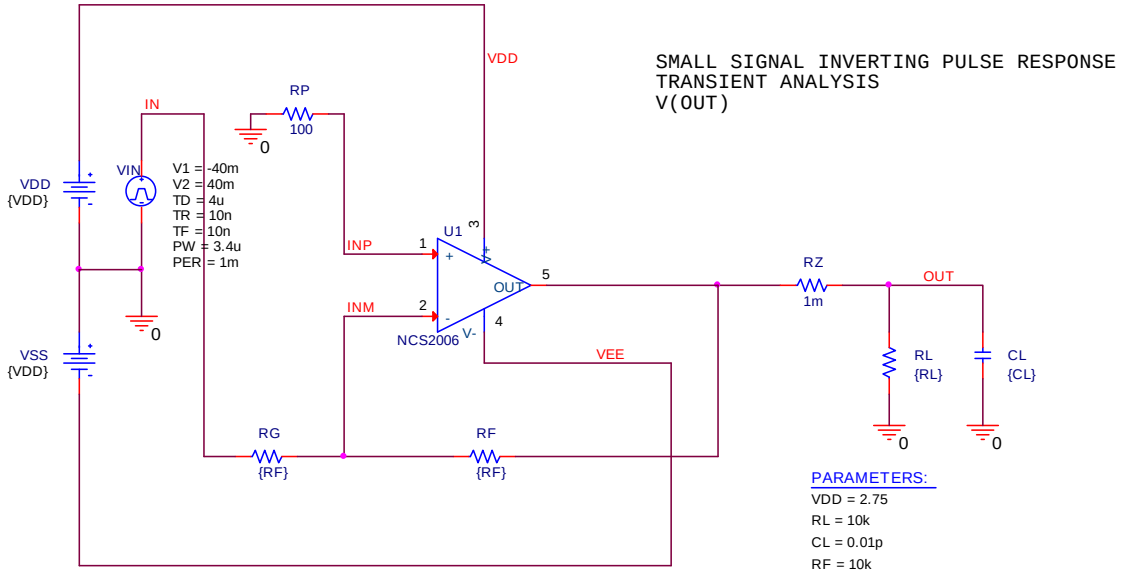

Figure 3-35 Small Signal Inverting Test Circuit

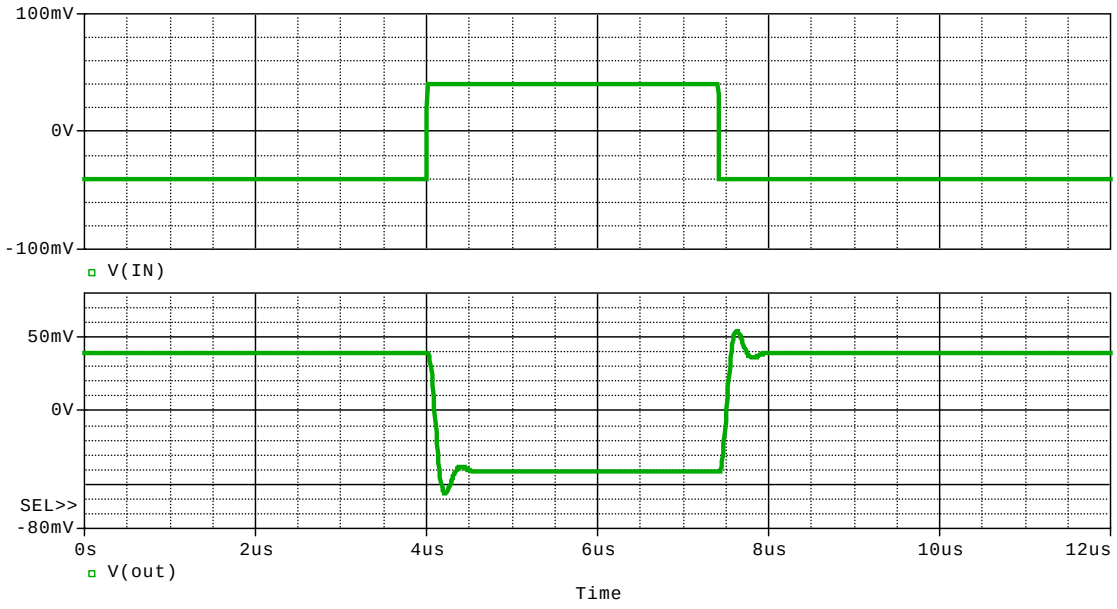

Figure 3-36 Small Signal Inverting Test Results

5.1.18 Large Signal Non-Inverting Pulse Response

16_LSPULSE

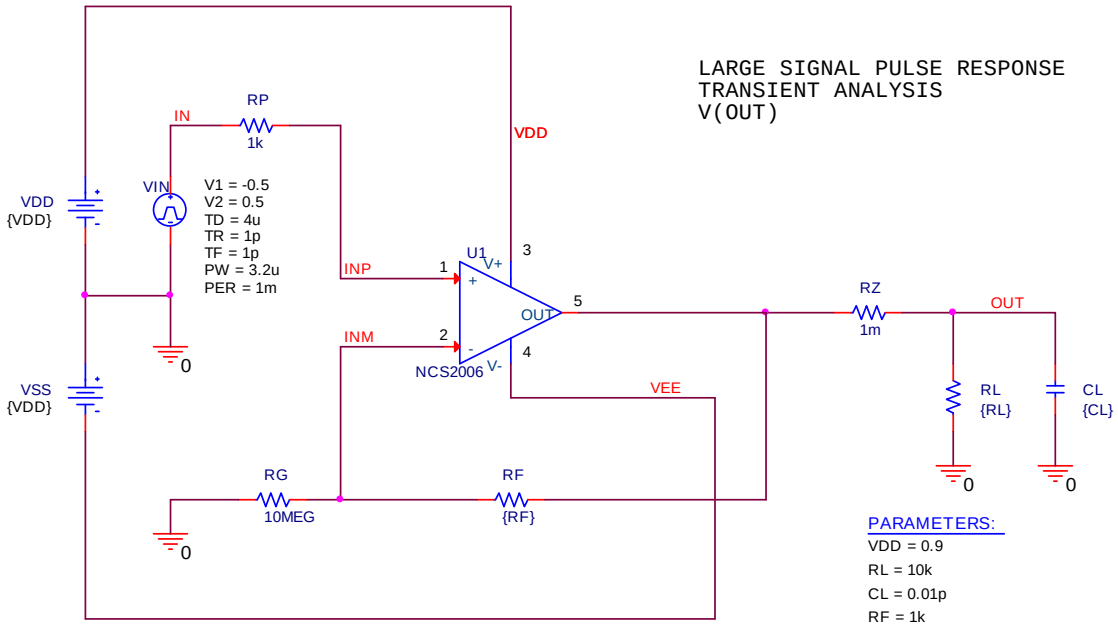

Figure 3-37 Large Signal Non-Inverting Test Circuit

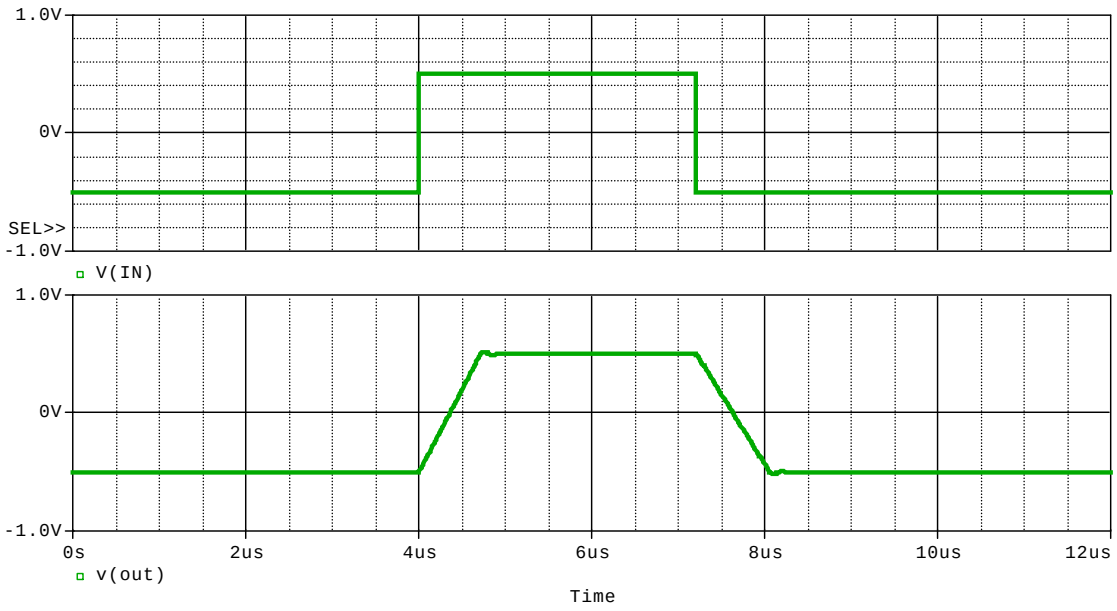

Figure 3-38 Large Signal Non-Inverting Test Results

5.1.19 Large Signal Inverting Pulse Response

16B_LSPULSE_INVERTING

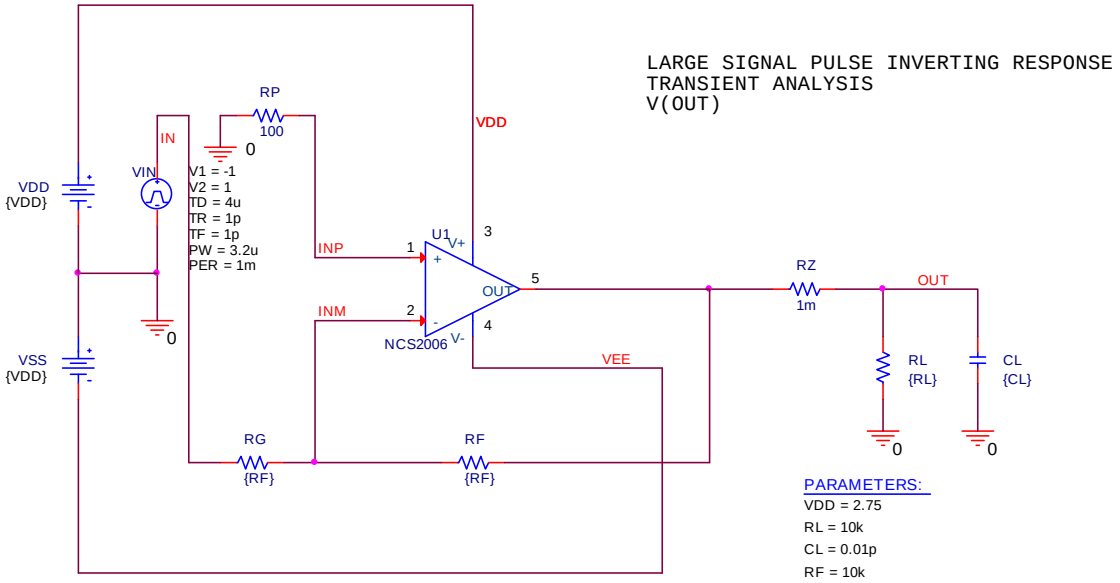

Figure 3-39 Large Signal Inverting Test Circuit

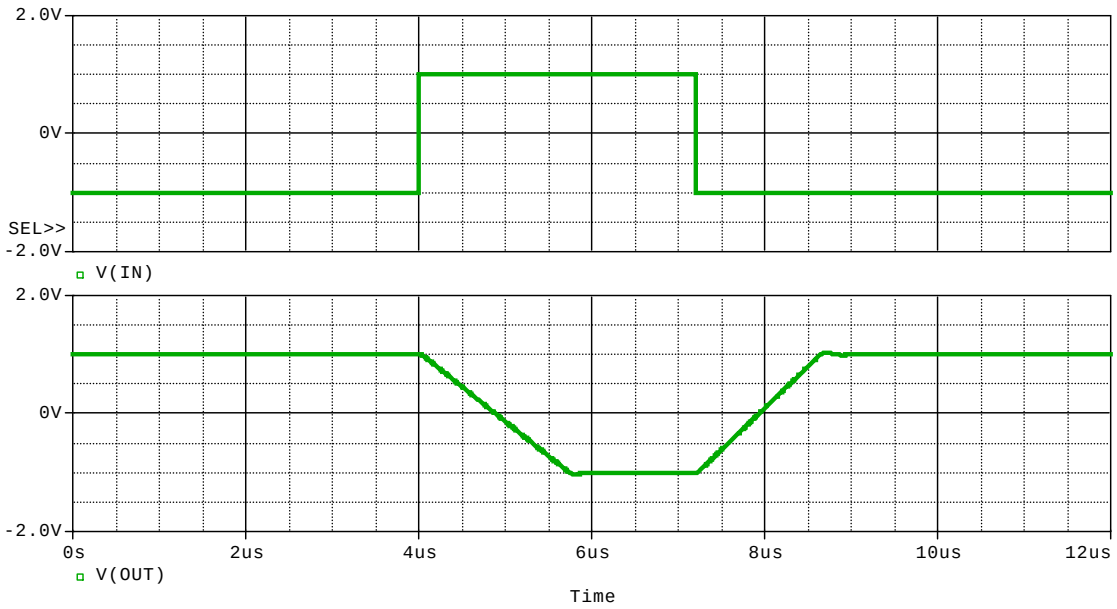

Figure 3-40 Large Signal Inverting Test Results

5.1.20 Quiescent Current vs. Temperature

17_IQUIESCENT

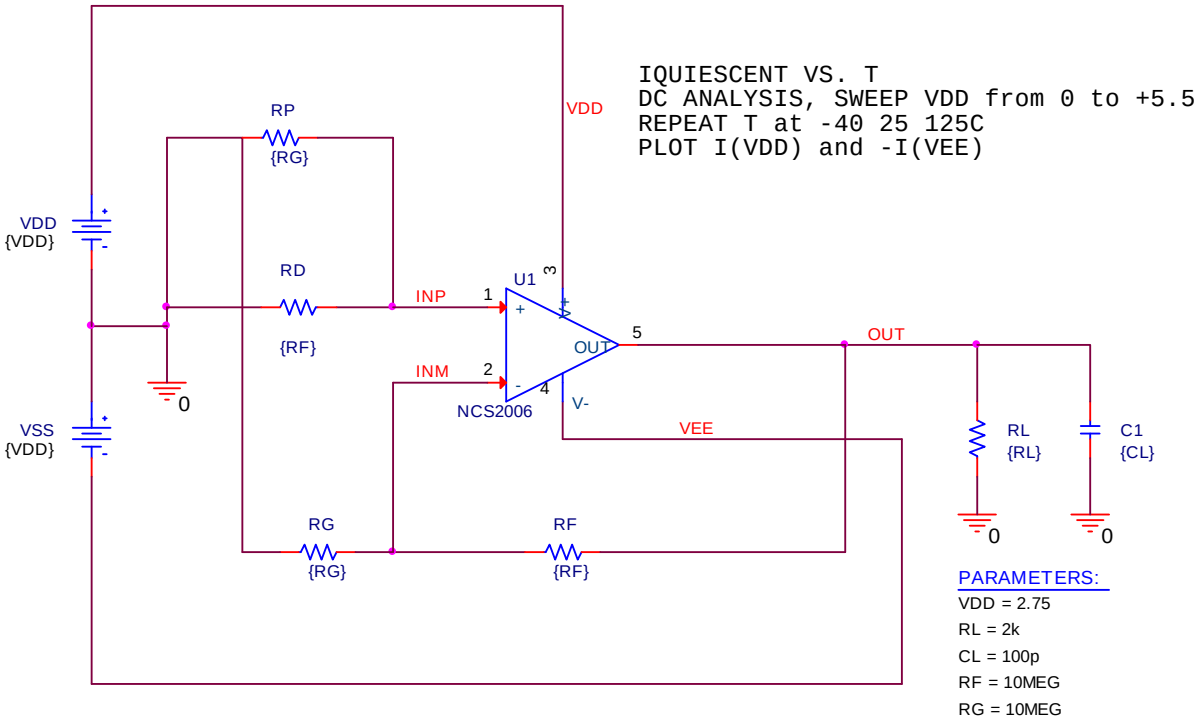

Figure 3-41 Quiescent Current vs. Temperature Test Circuit

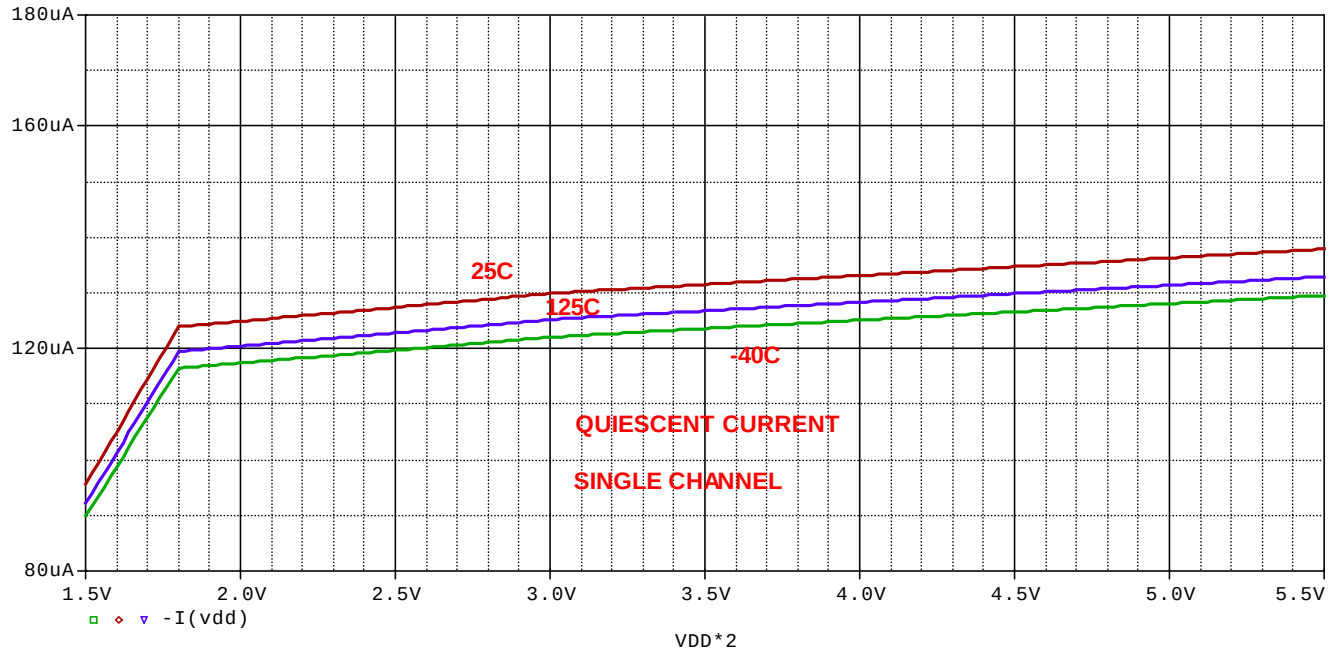

Figure 3-42 Quiescent Current vs. Temperature Test Results

5.1.21 AC Analysis with Noise

18_VNOISE

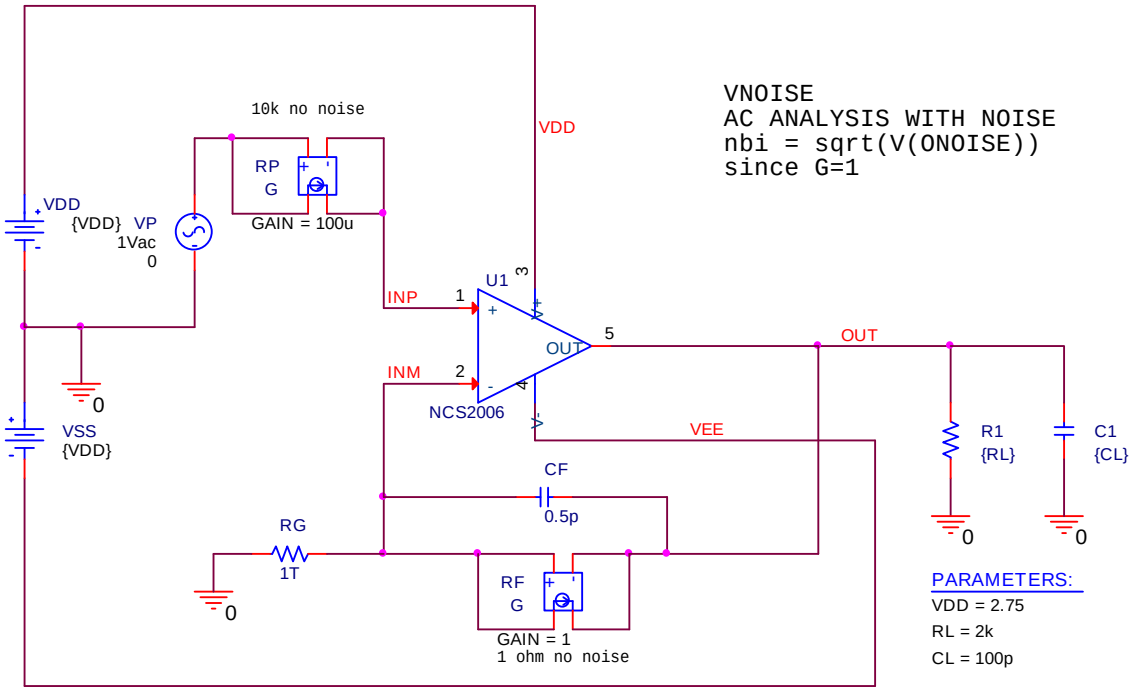

Figure 3-43 AC Analysis with Noise Test Circuit

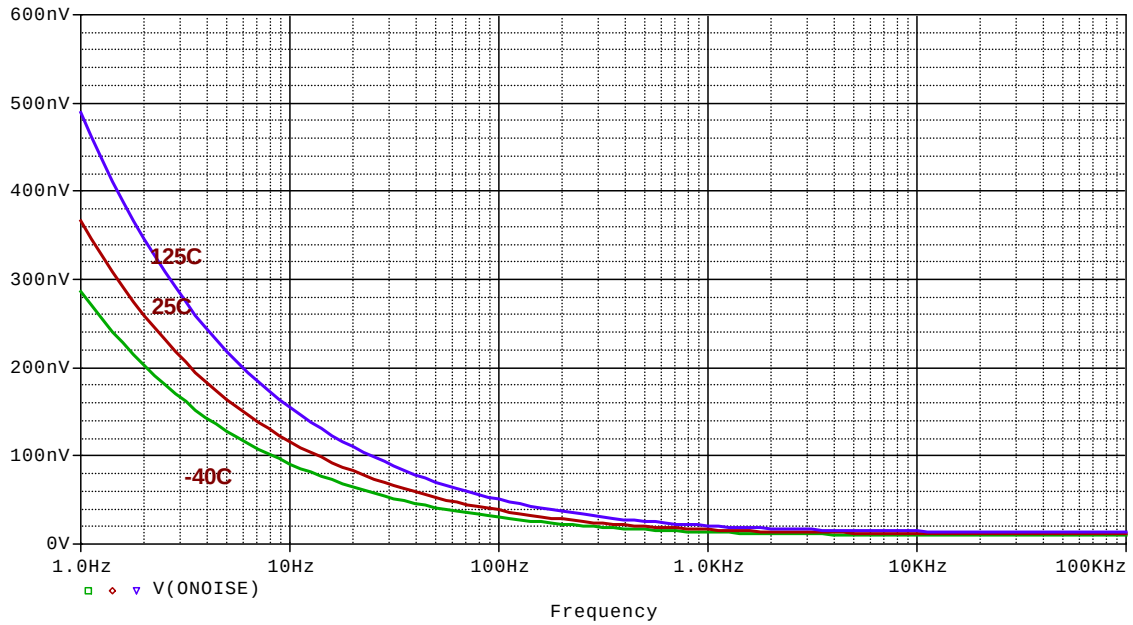

Figure 3-44 AC Analysis with Noise Test Results

5.1.22 VOS vs. Temperature

20_VOS_VS_T

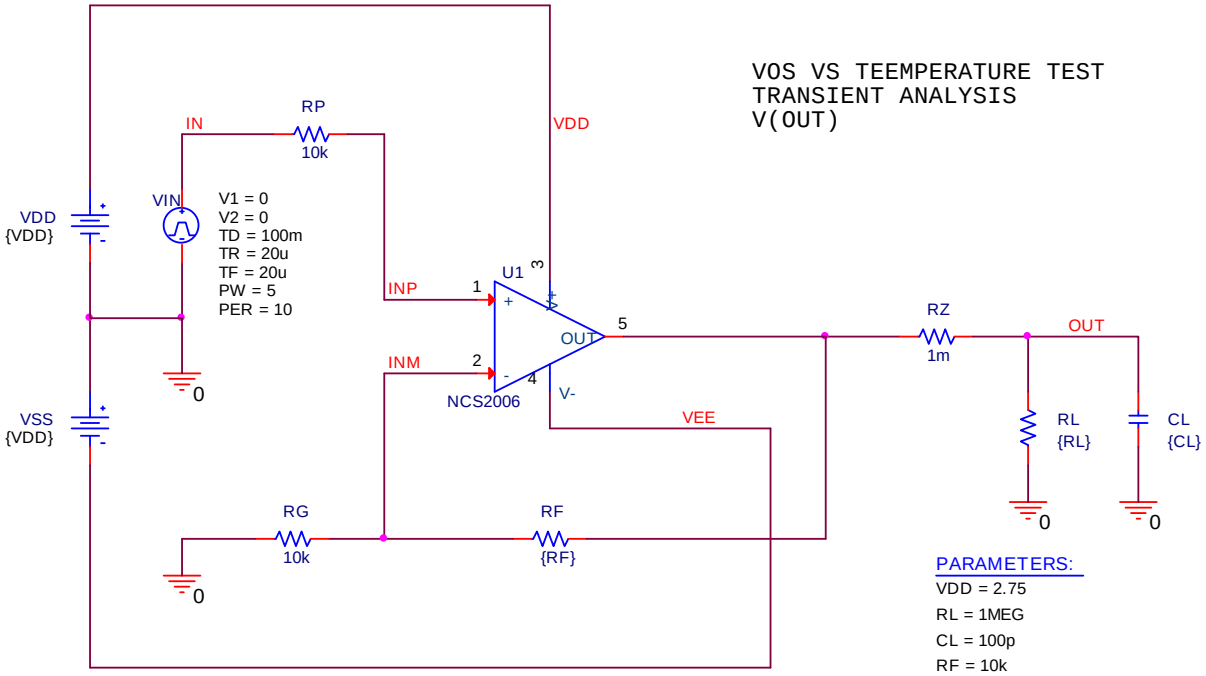

Figure 3-45 VOS vs. Temperature Test Circuit

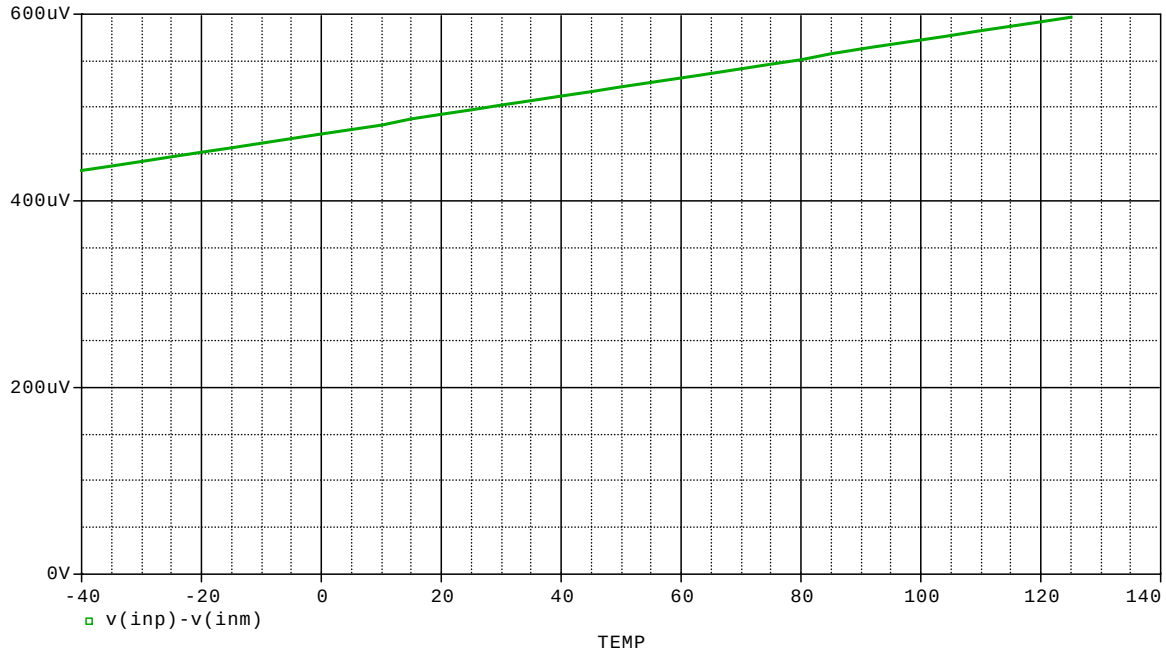

Figure 3-46 VOS vs. Temperature Test Results

5.1.23 Single Ended Pulse Response

21_SINGLE_ENDED_TEST

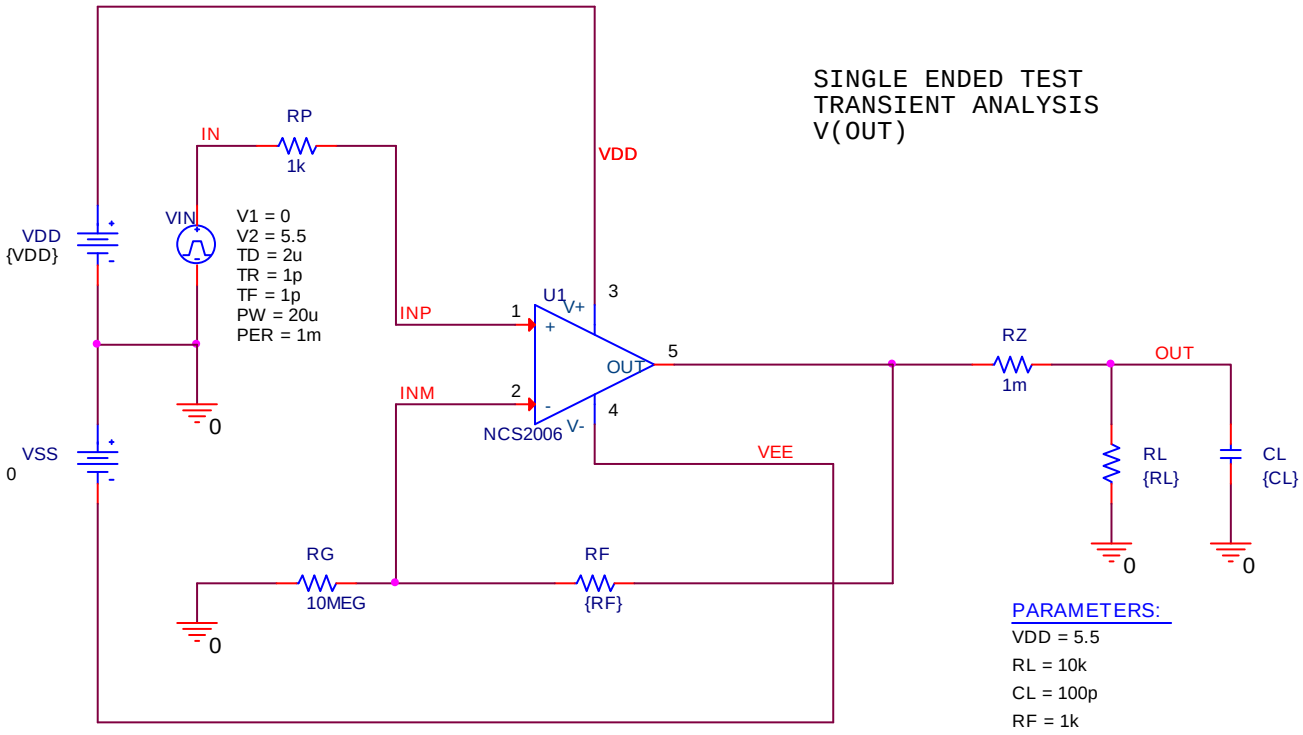

Figure 3-47 Single Ended Pulse Response Test Circuit

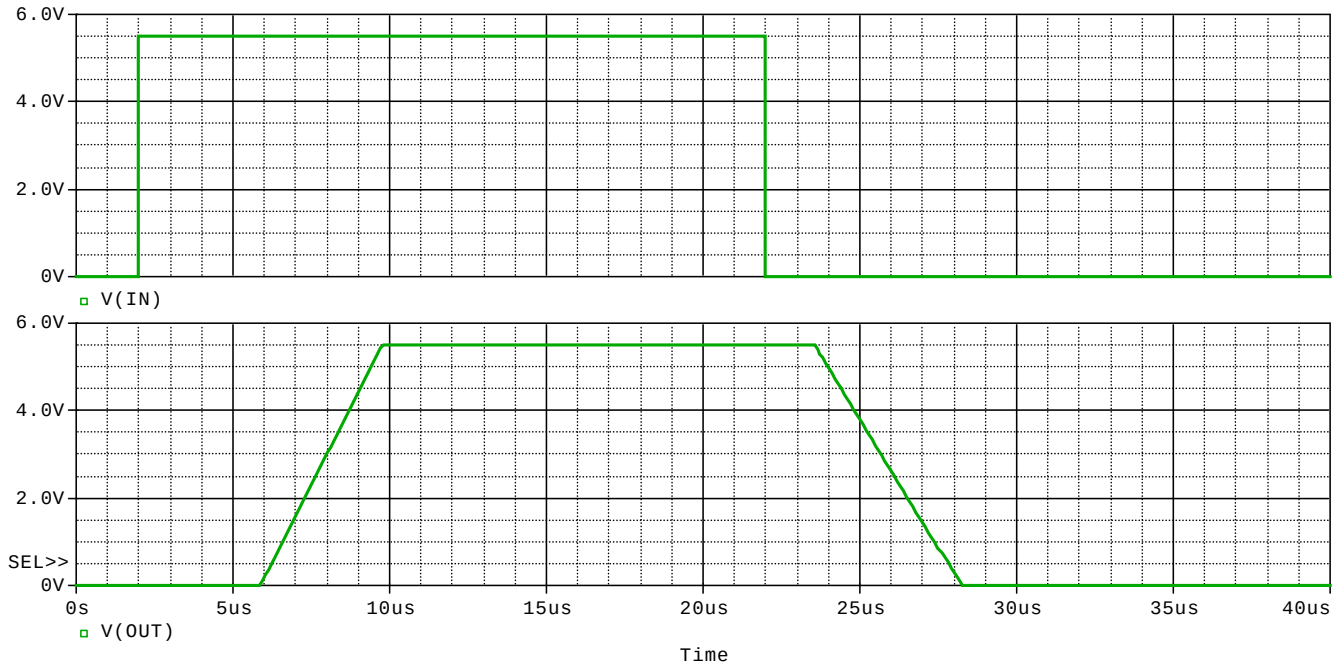

Figure 3-48 Single Ended Pulse Response Test Results

6.0 Model Verification Comments

Overall the results of the model verification testing shows good correlation to the results printed in the manufacturer's datasheet.

The model release includes both the NCS2006.LIB (SPICE netlist in PSpice format/syntax) and corresponding NCS2006.OLB (OrCAD Capture Symbol) file.

It should be noted that the model uses PSpice syntax and will NOT run in other SPICE programs. Error messages will result if the model is not properly translated.

The model uses various PSpice syntax extensions to model the opamp's behavior including math equations, LIMIT function, Resistor tempco, and TABLE models. These items will need to be translated into other syntaxes by AEi Systems, if customers request support for any other simulator (LTSpice, SIMPLIS, Microcap, Multisim, etc.).

Translation of the model is not permitted by anyone other than AEi Systems.

The CMRR is only valid to approximately 50kHz due to model topology limitations.

The input bias and input offset currents are shown to linearly increase with temperature as per the provided curves. Due to model limitations the input bias and offset currents increase exponentially in the model. The simulated currents at 125°C are in good agreement with the values in the curves.

The model does not emulate the output impedance variation due to the supply voltage changes. Output impedance curves are provided for Vs = 1.8V and Vs = 5.5V. A compromise is made by modeling the average of the two curves.

The gain bandwidth product (GBP) in the datasheet is stated to be 3MHz while the curve of the AC Gain/Phase provided shows a 4MHz GBP. The opamp model is set to match the 4MHz GBP shown in the curve. There's a compromise made between the phase margin and

gain margin with a simulated phase margin of 55 degrees and a simulated gain margin of 13.5dB vs. the datasheet specifying 60 degrees of phase margin and 10dB of gain margin

The offset voltage of the opamp is set to 500uV with an offset voltage drift of 1uV/°C as per the datasheet parameters. The offset voltage is not modeled based on the offset voltage vs. temperature curves provided in the datasheet.